STATUS OF IO PROJECTS AS OF APRIL 6

1. Micro: chasing bus errors problem. Seems to screw up when accessing on-board memory. Etched board being assembled, due here Wednesday.

2. Microcode: path to microvax almost solid. We have a workaround for the emulator problems. Need another PC to allow parallel development and debug.

3. CMI: wire-wrapped boards due in Wednesday. About 8 pals done, 20 to go. Working on CM IO Bus interface with Ed.

4. SCSI: microprocessor can access SCSI chips. Will try drive today then work on data board interface and buffer. Etched boards due Friday.

5. Data board: documentation updated. Etched boards due Friday.

6. CM IO Controller: register read/write came up over the weekend. (great work, Ed and Sandy !) Proceeding with debug.

7. Frame Buffer: board due in on Saturday, 4/11. John is programming pals. Simulation work is proceeding well in parallel.

8. Issues:

    We are hung out with only one DATA IO station. Both usage and potential impact of loss suggest we need another.

    Some parts shortages are going to cause minor problems and major stomach upsets. Paul and Bill have been doing a great job chasing material for us.

2/28 1 2 3 4 5 3/6 7 8 9 10 11 12 3/13 ... 3/20 21 ... 3/27 ... 4/3 ... 4/10 ... 4/17

α MATRIX (145)	10*	5*	20*	45	20	15	20	15	20	5		
α MICRO (12)			2*	10								
α Nexus (15)	3*		7*	5								
α Backplane (8) 8*												
β Matrix 1 (50) 10*	5*		10*	4*	21							
β MICRO (20)	1*		1*	1*	1* 1* 2*	1 1 1 1		(3)	(3)	(4)		
β Nexus (20)				1	2	3 4					(5)	
β MATRIX 2 (100)					Artwork		16 RAW BDS	(16)	30 (8)	(8)	30 (10)	(20)
β BKPLN ϕ (5) 5*												
β BKPLN 1 (25)	5*			5*		(10) (8)	(8)					

JIM

- 'I' * 'HW DEBUG' (2/1) ▲ COMPLETE TO (16/1) — Jim
- 3rd → 'K' 'MATRIX BD DEBUG' (1/1) ▲ COMPLETE TO MFG. ECCLES MATRIX
- 'A' (2/1) ▲ TO SW DEBUG 3rd floor
- 'J' 'MULTI-MICRO' TESTS (4/1) ▲ HW ENG TESTING TO (2/1) ▲ (TAKE MICRO TO 'L') MOSER
- 'B' * 'BACKPLANE TESTS' (16/1) ▲ complete (TO SW DEBUG 3/27 AS PINT) 3rd floor
- 'F' (2/1) ▲ FRAMEBUFFER DEBUG — 4/10
- 'G' (2/1) ▲ CMIO/HOLO - HW/SW DEBUG THIS WEEK 4/1 I/O
- 'D' (2/1) ▲ SW FRAME BUFFER DEBUG
- 3rd → 'L' (1/1) ▲ TO MFG MATRIX MATRIX
- 'C' 2/1 ▲ CMIO SW DEBUG
- 'E' (16/1) ▲ SPRINT DEBUG LAS NOW — John the sect breast office
- 'H' (1/1) ▲ I/O ENG DEBUG
- 'M' (1/1) ▲ MFG TEST

BETA SHOW QTR A — B B — N — μ(2) — START TESTING

QTR B — B B — N — μ(2)

- Diag
- Cable

5/11 with Tom Gby of AMD

16 bit micro controller 29116. – similar speed to 2910A.

Bipolar PROMs 2K x 8 – 27S291-ADC

2901D — 1st 1985 25% increase in performance

No future development for 2900, 2909/11. To be replaced by 2911? (availability unknown).

5/14

AMD questions:

1. min hold times, in general ← according to R. Rudis of AMD, should assume ½ of typical, or ⅓ of worst case.
2. Clock ↑ Sx time in 2909A
3. difference between Mich & Brick and data sheet on 2909A $C_n \rightarrow C_{n+4}$, Mich & B claim 9ns, DS claim 14 ns. use data sheet
4. PROM with pinout & second source 27S25 MMI
   PROM/EPROM compatibility physically not possible.

5/15

CS Memory: NMOS STATIC

4K x 4

IMS1420 (same as CM mem) 45, 55ns
Fujitsa MB8168
AMD

16K x 1

IMS1400 ? ns
MB8167A-45 45, 55
AM2167-45 45, 55

5/15 Danny, Bruce, Brewster, Carl

Discussion of information going from CU → CM:

Field	Size (bits)	Source (definite)	Source (maybe)
Address	12	ARG_M ; INC MOD_CNTR (MOD_CNTR + ARG)	ARG_M ; DEC, ADD LIT
Adr Flip	4	ADR<LSB> $\overline{\text{ADR<LSB>}}$	LIT
Chip Select	12	ARG	ARG_M ; INC LIT
Read/write	2	LIT	—
Flag	4	LIT	ARG
ALU	8	LIT 'ARG_M'	ARG
Inst Flip	4	LIT ADR<LSB> LIT<MSB> . MOD_CNTR<MSB>	ARG
OP	3	LIT	—
SENDR	2	LIT	—
LATCHTR	2	LIT	—
NEWS DIR	2	LIT	—
LATCH LED	1	LIT	—

LIT : literal from uC control store.

ARG : argument from FIFO, requires no modification.

ARG_M : " " " , " some " .

'ARG_M' : argument passed from FIFO to a shift reg, which is subsequently 'shift-mutated'.

MOD_CNTR : up counter with associated BOUND register. BOUND register loaded from LIT (message length dependent). Counter cleared by BOUND register load.

Notes:

1. In general there is only a single argument associated with each field. The exception is the address field, which has 2 or more arguments.

2. The flag field's components (FLAGR, COND & FLAGW) are all literals. For ROUTE, the CYCLE is either literal or 'XOR'. ?

3. The ALU field for LOADA & LOADB is either literal or 'ARG_M'. For store, it is literal only. For ROUTE, the CYCLE is either literal or 'XOR' (?), and the CHECK is 'ARG_M'.

may want to separate CYCLE & CHECK.

4. What about the READ & WRITE cycles?

   Ans. For READ, only the INST FLIP field is meaningful, the rest of the instruction is don't care.

   For write, 16 bits of write data is sourced from ARG, and passed as instruction.

5. CYCLE field is counted up from 0 thru 63 during route. The debate is whether this should be done by straight line ucode, or done via a ucode loop with an external HW CYCLE counter.

5/18

Mod counter & 'ARG_M'.

1) Mod counter is 12 bit HOLD/LD (from FIFO)/CNT (up only?) totally under ucode control. No need for status detection, other than completion of count.

Implementation will be much simpler if this is a down counter (no need for a comparator). Is this feasible?

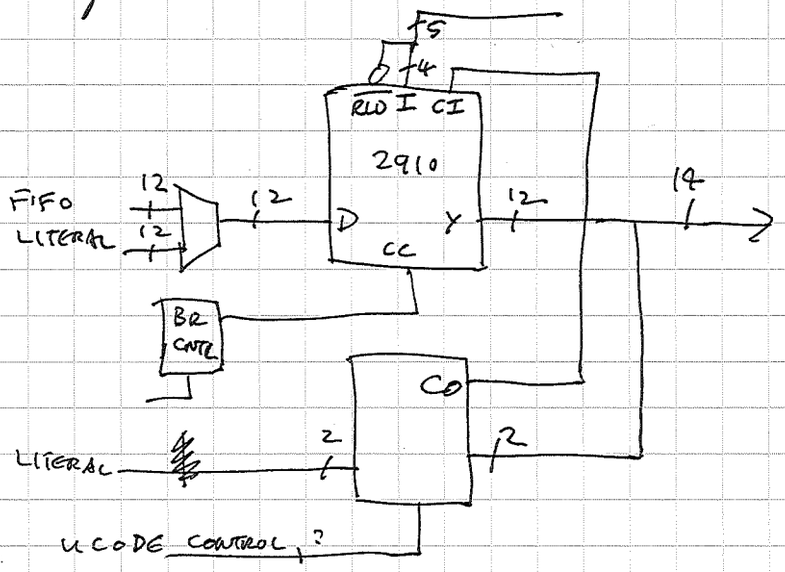
2) 'ARG_M' is actually a shifter and a mux. The shifter (16 bits) is loadable from the FIFO and does LSB → MSB shifts (both under ucode control). (HOLD/LD/SHIFT). The MSB is a branch condition to the ucode sequencer. It is also enabled by ucode to control the ALU mux selection.

This same shifter may be considered to be used as the receiver of the GLOBAL signal from CM.

The ALU mux has at least two inputs: literal ALU field from UW, or literal ALU field swapped (either nibble, or bit pair). A third input may be the CHECK field for ROUTE op. (CHECKing BANKS).

5/21

Consideration of 2910 as sequencer. Problem is the 4K addressing constraint. To overcome this can use one of two methods. One is ~~to~~ to have multiple 4K banks switchable under mode control and/or via FIFO dispatch. Another is to ~~branch~~ add a simple external 2 LSB address generator:



The big plus of using the 2910 is higher speed and smaller chip count. The minus are ucode complexity and constraints.

Higher speed may be meaningless if in a 2-stage pipe, the DP stage is slower. Chip count is in effect the only concern.

Ucode complexity/constraints:

1. no multiway branch (actually no trap capability). Lack of multiway branch is only a matter of efficiency. Lack of trap is binary. But if the only trap needed is due to HW error, then the sequencer ~~does not~~ need only be stopped ~~and~~. The implication is error/status handling is not done by sequencer, but by other hardwired logic. Also implies sequencer need to be revived after ~~that~~ being stopped.

   If multiway branch is indeed needed, can implement via JMP MAP or COND JMP VECT. (??)

2. Loop counter can do both single instruction or loop iteration. Not a concern.

3. Ucode flow control must be done @ 2LSB = ØØ boundary. This is necessary to keep the stack push/pop to occur only when the 2LSB = ØØ.

The PC ~~only~~ is incremented only when the 2LSB overflows.

Branch ?? Branch does not need to occur @ 2LSB=ØØ boundary. In fact, will use the 2LSB for multiway branch.

It seems like the micro assembler must have the smarts to identify the 2LSB=ØØ state.

5/22

Booting: CS load can occur either ~~during~~ after power on, or 'on line'. The HM will issue a BOOT instruction with the following arguments:

OP = BOOT
~~ARG1~~ ARG1 = LAST
ARG2 = SIZE
ARG3 = SA
ARG4 ~~= ARG4~~ LSB
5
6
7
8
9 MSB
} uw data
.
.
.
ARG N

LAST indicates whether this is the last of a series of BOOT instruction. UC saves this bit for determining whether BOOTing is completed or not.

SIZE each BOOT instruction can boot up to 4K of uw.

SA starting address of SIZE

uw data each uw is divided into 16 bit words. For a 96 bit wide uw, there will be 6 16-bit words for each uw load. LSB 16 bit word is arbitrarily selected as 1st word passed.

After HM issues a BOOT instruction with LAST set, it can read a status bit BOOT DONE to determine if BOOT is completed.

On the UC side, the BOOT instruction is handled by PROM code. PROM/RAM selection is controlled by power on and ucode. After an initial power on, PROM is enabled to handle booting. ~~During~~ For After booting is completed, the PROM code will enable RAM selection. For on line booting, RAM ucode will enable PROM selection ~~and~~ to execute the boot routine.

The PROM code goes thru the following sequence:

1. saves LAST bit via a BOOT CNTL field, which has the following function:

   NOP
   LD LAST CLR BOOT DONE
   SET ~~BOOT~~ BOOT DONE, CLR LAST

2. saves SIZE in the LOOP counter of 2910.
3. saves SA in PC of 2910
4. writes RAM using the WE CNTL field. The last 16 bit width of a uw also increments PC and decrements LOOP.
5. continues writing until LOOP zeros out.
6. if LAST was not set, then continues waiting for the next BOOT instruction.
7. if LAST was set, then use the BOOT CNTL field to set BOOT DONE and clear LAST.
8. Enables RAM selection.

5/22

Valid meeting. Rich (from Valid), John, Dave

① HW DR11-W interface to VAX.

End of wk - ship by Friday
Month - 2 wks.

SW 2,500 product #2360
5000 compiler
25000 timing verifier
5000 postprocessor
25000 logic simulation
HW 64,000 (instead of 69,500)

Streaming tape.

discount difference for system II - due to cost.

System 19,500 + ½ MB (4000) + SW licenses (for 2nd only)

② Device library.

③ Memory size & mass storage vs database
70 MB ~ deemed sufficient

AMD — 200 units within 2 yrs.

5/24

Versatec 8236-F electrostatic B size @ TMC

Fleet Lease - purchase

Compiler 5 min
Packager 5-8 min. } for a 300 IC board, single user on system 1.

2-5 times faster on VAX for simulation.

Valid questions.

1. PAL20 library: will it include test vector simulation?
   What is interface (HW & SW) to data I/O?
   Actually, PALASM functionality comparison?

2. AS & ALS library availability.

3. Versatec plotter: HW interface
   SW driver

4. Serial interface to VAX/LISP: HW: RS232 port?
   SW: UL/DL.

option

ALS library available in 6 wks 31 parts
AS only 4 parts available ??

PAL20 library not available till Sept.

Valid supports Versatec 36" plotter, but not "40".
Will require parallel interface ($6400)!

available by end of June.
1ST of June

5/29

HOST MACHINE interface issues:

1. Ideally CM should appear to HM as a combination of memory & memory-mapped I/O registers. This may be a problem because BI is separated into memory or I/O, while 3600 is either memory, M-M I/O or DMA.

2. Do we need to synchronize CM clocks with HM clocks?

3. Is there a need for a pipe stage between HM and CM FIFO?

4. 3600 only has 24 bit address. After 5 bits are spent for board ID, there is only 19 bits to address up to 1/2 M× per board.

10

5/30

Fairchild

F starts in South Portland Maine (also for LS)

2×10^6 devices / ~~week~~ by end of year.

Hamilton largest Fairchild distributor, gets 30% of production.

F245 has 50% yield, and backlog.

Committed thru '85

Barry Davison Sales manager for Tele-Comm / computer segment
$250K - 500K OEM break point.

29Fxx spec sheets.

Also 4K x 4, 16K x 1 Static record sourcing IMS.

74Fxx - PC plastic commercial, always burnt in (sometimes tested) by distributor.

- PCQR Tested in Fairchild factory.

5/30

	Processor	Memory
Per CM Board	16/chip × 32 chip = 512	4K bit/processor × 512 = 2M bit = 256K byte = 128K wd = 64K LW
Per ¼ machine	512 × 32 = 16K	256K byte × 32 = 8M byte = 4M wd = 2M LW
Per machine	16K × 4 = 64K	8M byte × 4 = 32M byte = 16M wd = 8M LW

Memory access issues:

1. Currently ~~the~~ coming from HSR there are 12 chip sel bits and 12 addr bits. ~~The 4 LSB~~ This allows addressing up to 16M x of memory (24 bits of addr). I presume x = wd. The LSB 4 bits of addr also forms the addr flip bits. How are these 28 bits of info distributed thru out the machine?

2. How wide is the data path? It is definitely 16 bits wide between uc & Car. Should we make it 32 between uc & HSR. (The ~~FIFO~~ Input FIFO is 32).

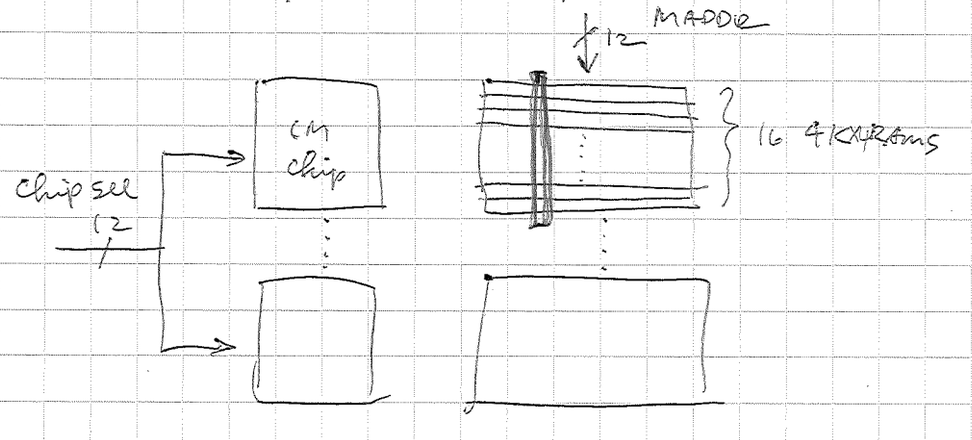
3. Where do the 16 bits come from? Within the 4K attached to each processor, or scattered?

4. How is parity handled?

5. Some of these questions, once answered, will help decide whether direct R/W should go thru the FIFO or not. Implementation-wise going thru the FIFO is much simpler. But is only efficient in handling block move.

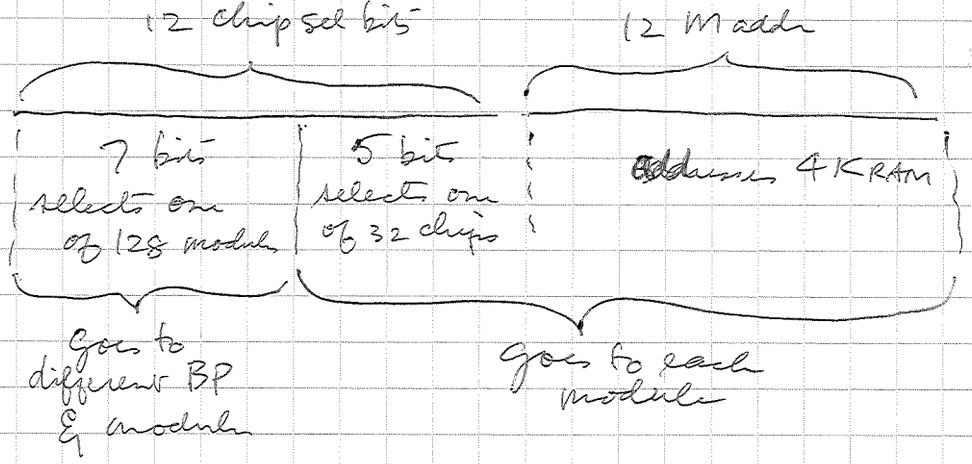
Some answers from Bruce:

The 12 chip sel bits selects one of 4K chips within the whole machine. The 12 addr bits select a bit of 4K ram chip attached to each processor. A 16 bit memory access R/W is address one particular chip, and 16 bits of Rom data, one coming from each 4K RAM attached to one of the 16 processors within the processor chip.



incorrect.

The 4 flip bits will magically allow 16 bits to be read of a single 4K RAM chip attached to a single processor. Write operation, however, cannot take place in a similar manner.



3/31

CD /CM/DOC/...
LS
CAT filename | more
CD /U/CLCM
control D to logoff

Symbolics questions

1) Data size = 32 bit only?
2) Timing relationship between FIRST HALF & CLK
3) Is clock variable cycle time?
4) "Wait" applies only to Memory devices?
5) ECC correction, always right back regardless of correction or not?
6) "With ECC" only applies to Memory devices?
7) what is the ±D ROM content?
8) Block move operation? yes but just means copying.
9) "SPY" necessity?
10) Trap handling by LBUS device.
11) For a CM, is there implication of microcode change?
12) CM → MEM operation, how is ECC handled?
13) How is BLOCK REQUEST related to this?

6/1 Symbolics meeting with Chas Howath & Bruce Edwards

Block mode restriction - no page boundary crossing.
256 word page size.

SPY bus - no need to interface

FH drive LBus for first half for mem mapped and ~~IO~~ IO

Memory

LB write
request
wait
Addr <0:23>

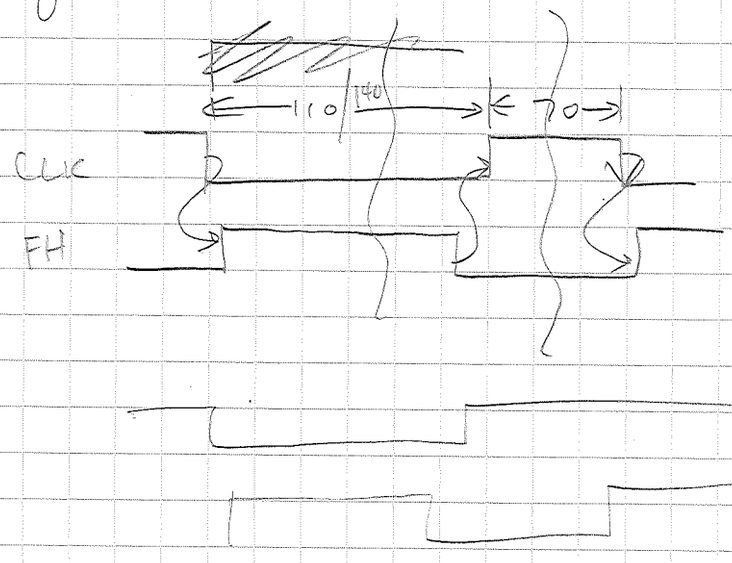
Udevice

LB Dev Read
Write
<0:9>
Dev COND ← 1 on wait req.

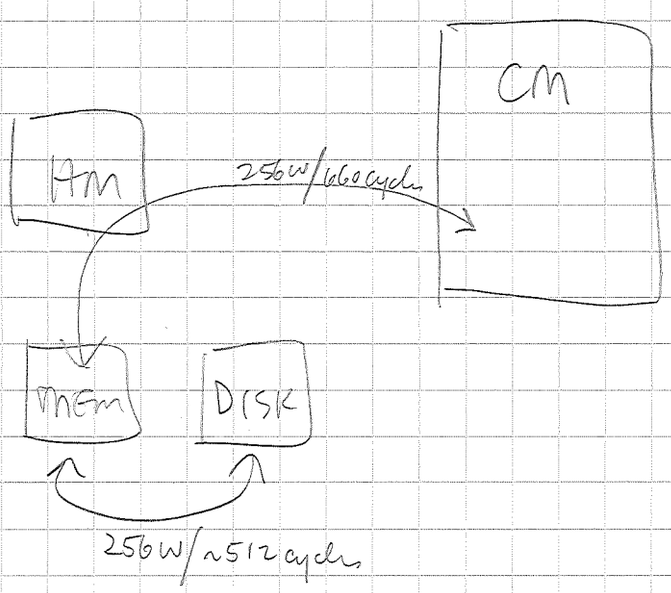
Wait & write ecc applies both to mem & udevices.

Clock is variable cycle:

fastest:



WAIT etc should be driven @ clock edge.



256K Memory board
I/O Board

Ucode support.

6/4 Augat

Custom - 10 wk lead time
4 wk design
6 wk fabrication.

Solder mask on V & G optional.

	G/G	G/T	
PG314	1.4	1.1	1-4
	1-2	1.0	5-9

C410C103M5R5CA .01 mf cap recommended
KEMAT

6/5

SW8 on CPU board away from hd gets auto boot

6/6 LMI

Disk 15Mbit rate.

George White @ TI Irwin
714-660-8207

NM Bus spec.

6/7

C. Horvath from Symbolics suggest for blocks more than FIFO make FIFO address appear as a 256-32 bit adr page. This will allow disk DMA directly into FIFO.

→ Mark Thayer Augat CAD engineer.

Design Review on custom board — week of 18th.

ASCII characters in Net list

Thomlin hook up to Attleboro, Augat will post process.

Documentation:

Bob Hureault

3/12/313 4 on shelf 1405
3 wks lead time

WW $251 est. 2500 wire.

Online / Controller
Normal / Auto   Contrast control
LID open + LID safety
6 paper

For more Expan [New toner type H   4 bottle
Concentrate " "   2 bottle
Clean   2 bottle

posit
origi
with
both

pin

GDD
USE MISC

GD 4501.BODY

GRID .05 1
LF2 (WIN FIT)

WIN (down)

position origin within body
- Smash origin
- delete
- Add origin

alternative is to create whole body as group and then move over to origin

Add DOTS @ end of .1" wire or Bubble (.05" radius circle)

CLK △ use green 3 trim

Note all pins with body

DIS .05 all notes

GRID .025 2 to center note with pin

GRID .05 2

pin NAME ↘ pin about

SIGNAME all pins.

Check via LF4, LF6

WR writes

Gd _ . PART

add defin
drawing

Property Title 4501
Abbrev
primitive = true

WR

Gd _ . LOGIC

Add 4501 and place @ origin

Add pin property @ each pin (w/G button)
PIN_NUMBER (pin#)
INPUT_LOAD (1,-2)
OUTPUT_LOAD (-1,2)

Add Body property (y button)
POWER_PINS (VCC: 2Φ, GND: 1Φ)
SIZE 1

Check to show attachments & props.

SIGNAME

this is the way to go 6/26

UA can be placed & read in a similar manner (this allows PE handling by PROM

1. need uw reg to hold shifted fields from RAM array.
2. can't read PROMs in parallel.

6/25

Control store verification: Not quite

1. HM writes Status reg to put uc in diag mode.
   This basically a) NOPs commands to CM.
   b.) defaults OF mux control to diag sel.

2. reading of RAM array is controlled by PROM code, & vice versa

3. for each RAM CS address read, PROM code will control OF mux sel, and write 3 32-bit entries from CS into OF.

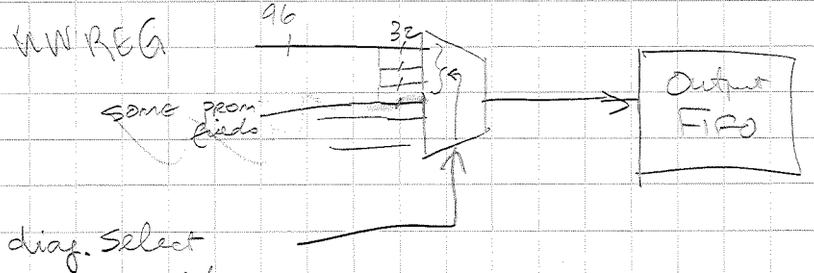
4. PROM code read is similar (1 32-entry / PROM address)

5. Block read is possible

6. need to inhibit parity check on GBUS.

7. after read is complete, control always returns to ROM.

8. HM reads OF & clear diag mode bit.



6/26

Error handling:

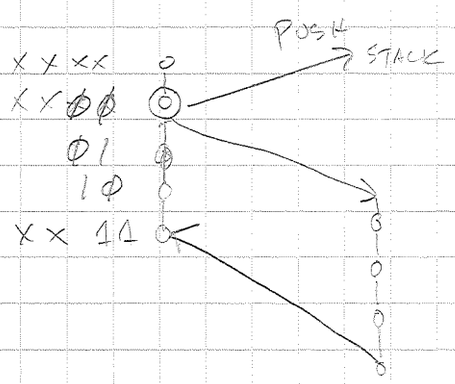
In general a HW error will stop machine operation (NOP) & will preserve the error scenario. Error bits are set in status register. HW reads all error info & resets CM.

There are 4 HW error detection mechanisms:
1. ~~[illegible]~~ error from CM
2. Parity error of CS.
3. Parity error of IF
4. " " " CM return data

6/27

Brad's suggestion for handling the LSB in UA:

Place no restriction on where subroutine calling occurs (i.e PUSH stack). Return will always go back to XX11.



@ MISC directory
VI COMPILER.CMD

Change root directory to 'IC'

Candidates for branch conditions & Status bits.

Branch Conditions	Status
- GLOBAL	GLOBAL
- SAVED GLOBAL	SAVED GLOBAL
- ERROR	ERROR
—	IFIR
- IFOR	IFOR
- OFIR	OFIR
- —	OFOR
- STK FULL	STK FULL
- ADDR ZERO	—
	CS PE
	IF PE
	CM DATA PE
	CM DATA W0 PAR
	CM DATA W1 PAR

6/30

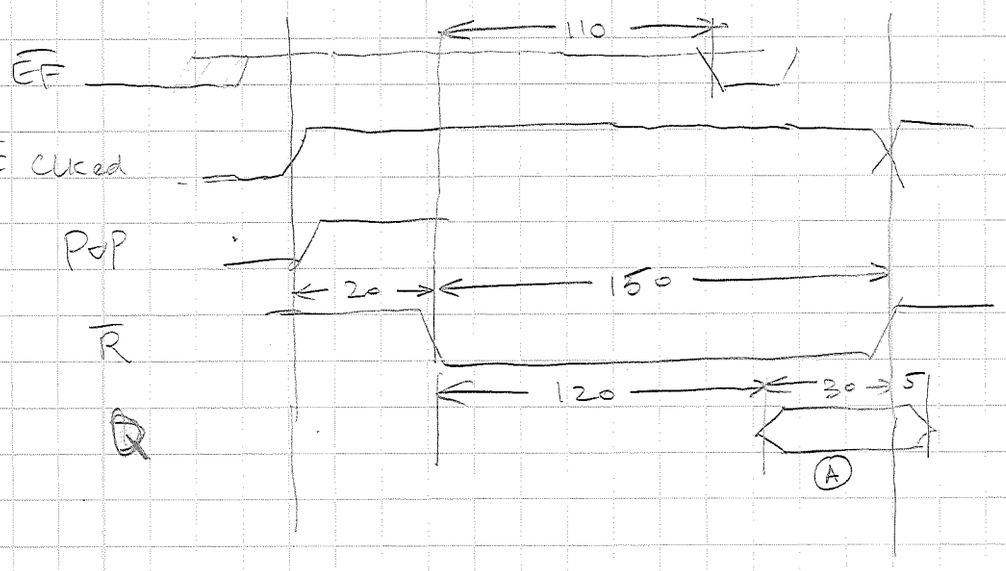
Bus error handling on LBUS, more presently.

Potential solution by Chas Howard. Add wire on DP board (COND). Signal to be driven by CM. Generate special MCode for CM/LBUS Xfer code and monitor (COND)

Reading IF by HM.

1. HM stops UC
2. HM sets DIAG — switches IF output clocking.
3. HM reads IFOR from Status Reg.
4. HM reads IF

7/4. IF timing



1. Ld & POP within same cycle is worst case.
   (A) time (about 30) is needed for Parity check and/or write data framing.
   Cycle time ≥ 170
2. if cycle time allows for Ld & POP, then back to back POPs is no problem

Questions for MOSTEK

1. Does $\overline{EF}$ toggle after 1st read if >1 entries inside?
   If it does, how long does $\overline{EF}$ deassert?
   (similar questions for $\overline{FF}$) ← MOSTEK says will not toggle 6/6

2. Does $\overline{EF}$ have min pulse width spec? i.e. if R & W co-incident. (same for $\overline{FF}$) ← MOSTEK says NO!

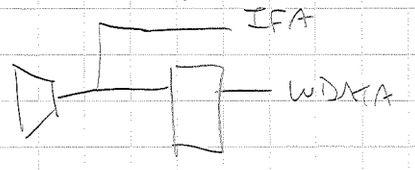
3. If $\overline{EF}$ & $\overline{FF}$ are edge triggered by $\overline{R}$ & $\overline{W}$ (as specced), can $\overline{R}$ be asserted all the time so that Q is valid after the 1st $\overline{W}$.
   i.e. does Q need a low going edge of $\overline{R}$ to become valid?
   MOSTEK SAYS YES, Q is edge triggered.

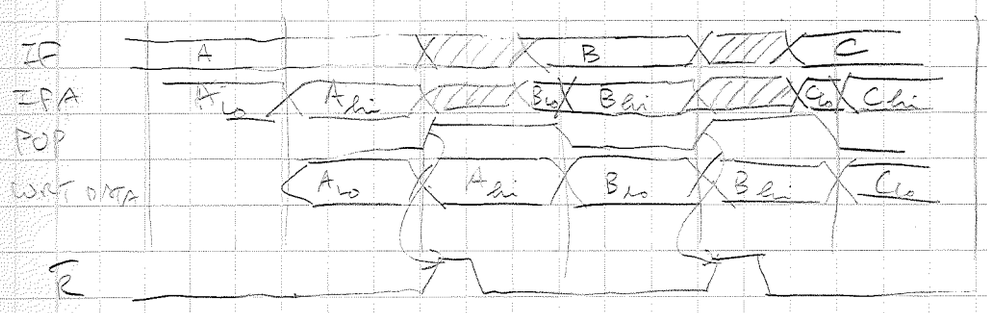
this scheme does not work,

Read sequence is:
1. check EF
2. create R
3. leave R low until read is done
4. deassert R

every other cycle

Need holding register for WR data in order to do back to back "IF" POP's





Micro sequencer timing.

D → y → accum

10	15	20	6.5	55	2	= 108.5
F374	F157	2910A	F244	RAM	set up F374	

I → y → accum

10		35	6.5	55	2	= 108.5
F374		2910A	F244	RAM	set up F374	

DP timing

Worst case is IFLIP from ADDR

		D→P6			15			
10	15	30	9	22	8	34	2	(145)
F374	F157	2904C	2904	2901	F157	F280	tsu	
						x2	F374	

F153

86 →

Can be
F280 x2 + F86
= 25

IFLIP bits

Wait

0	0	literal
0	1	Madder
1	0	Madder ! modcnt
1	1	literal ⊕ Madder

4/23

	25	25	25	34	2
AS08	PAL	PAL	PAL	F280 x2	tsu F374

←

7/9

Single Stepping:

Single stepping may apply to machine cycle or macro-inst cycle. To be able to do either (or even both) seems insufficient. The info at each step is either too fine or too coarse.

SS is not needed for loop back test, nor is it needed for mode debug. Won't be implemented.

9/10 result of design review

aw expansion:

1. add extra branch control bit.
2. add hold bit to hold uA, uW & INST register for loop back. It will also halt uc. To be reset by HM (HM RST?)
3. add SEL HM INST to allow an instruction argument to be passed. This is a 2-bit field for STATE and SEL.
4. add invalidate parity bit ~~for~~ for bad return data parity. save in OF.

HW addition

1. add separate 2910 ~~for~~ for PROM sequencing.
2. add SAMPLE bit in STATUS REG 0 to allow HM saving uA randomly.
3. ~~add CLEAR~~ add holding reg (and mux log) for inst. argument.
4. expand branch control.

LW width

84 committed + 3 (?) ALU comments + 5 (design review) = 91

Often Hw added..

1. ex-OR of MADDR and FFLIP

2. trap logic for RST, ERROR

Resistor, diode

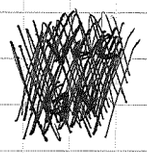
SOHRAB ABADIAN

1. No assertion check

2. 7.0 will fix

TOM LUI

1.



Bus

PIN_NUMBER (<msb, lsb>)

PIN_NAME A <msb:lsb>

30

TED BILODEAU 535 Sudbury Rd
Concord

369 1238
& 1796

CAT FILE ~~DRUM~~/TTYA

AUTOMATED SYSTEMS INC.
The Total Concept Company
1505 COMMERCE AVENUE • BROOKFIELD, WISCONSIN 53005 • PHONE (414) 784-6400

March 10, 1987

Clem Liu - Project Manager
Thinking Machine
245 First Street
Cambridge, MA 02142

Dear Clem,

I would like to address the problem encountered on your Beta Matrix Board. The major problem we faced was sparatic unetched copper in ground and power plane clearances and trace to trace shorts. This has been a problem in other products but not as prevalent as on your boards, this is due to the card being so large and dense. The problem is caused by photoresist being polymerized on the edge of the inner layers. This resist chips and flakes in the developing operation. Because the resist is polymerized it does not dissolve in the develop operation but does however become very adherent as it is being recirculated in the developer. If these chips land on a clearance or between traces, they tend to adhere very well and subsequently do not allow etchant to attack that particular area. These defects are very difficult to see because they may be extremely small yet still allow copper to connect to the plane.

We resolved this by splicing opaque borders on to the inner layer A/W so no photoresist becomes polymerized. Also, the developing sump, rinse, and exit rollers have been thoroughly stripped.

As a result, we have minimized these defects and inner layer yields have increased substantially. If any further explanation is necessary, please do not hesitate to call.

Your truly,

AUTOMATED SYSTEMS, INC.

Don Dawson
Special Project Manager

DD:lj

cc: Kim Nap
Mike Wilson
Mike Taplin
Bob Wandtke

Chas H. & Bruce E. Kris Kam.
@ Symbolics

FEP reads ID PROM, passes onto LISP prog. for configuration.

(ID PROM should signal different memory sizes).

Physical slot represents memory map I/O reg #.

Augat SCH131-2 -3 WW board.

Extender Boards. ← crystal change for clock slow down.
Connectors. will run @ speed with extender in.
stiffeners.

Cabling to CM. from BP.

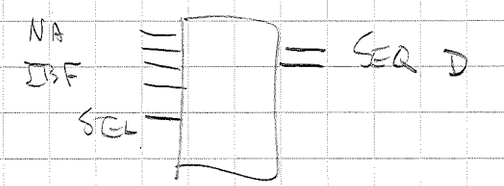
Paddle card. WW info.

Valid John Ludgey

Shrink:

(1) SEQ...1

use PAL for 2 bits of SEQ D



prob: slow

gain ~ 1/2 PAL

(2) SEQ...1

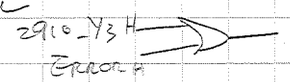
get rid of UA E & F

gain: 4 Freq
prob: each UAx drives 24 (instead of 16) ROMs

(3) SEQ...2.

2 solutions ~~of~~

1. generate same trap addr for both error & trap
2. use



gain: Y2 Freq
prob: slower. - not by much

(4) CS ... 3

SAVED UA use F374 & UW CLK A HI & ~~[illegible]~~
Change SAVED SPARE A<2:0> to <1:0>, ~~[illegible]~~ Change
UW FROM SPARE <1:0> to <2:0>

Gain: Saves 1 S374.
Prob: spare distribution less flexible.

(5) CS ... 4.

2 solutions:

1. One version of WE
   Gain: 1/2 F244
   Prob: each WE drives 32 RAMs

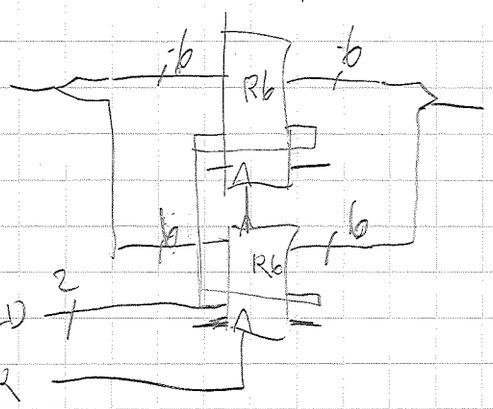
2. use PAL
   gain: produce gen gate & 1/2 dip.
   Prob: big skew, may be no concern.

(6) DP: ... 1

use 2 PALS for loading MOD_REG.

Gain: SOME PAL SPACE, no need to gate clk & gen ld signal

F48



~~[illegible]~~

(7) DP ... 1.

~~Obs~~ use 2 PMCs instead of 3 MCS69

Gain: 1 MCS69, convol decoding.
Prob: PMC fit.

(8) DP ... 1

use 2 PMCs instead of 3 FIG1.

Gain: 1 FIG1, convol decoding.
Prob: PMC fit, slow.

Reading IF:

Original idea is to allow HM read IF directly. This implies switching IF read clk from UC clk to GBUS clk. Implementation of this scheme turns out to be non-trivial.

An alternative is to allow HM read IF via a macro. Scenario is: UC is stopped (only RAM seq, but not PROM seq). IF READ macro is dispatched to PROM code, which reads IF and dumps into OF. HM reads OF, reads IFOR and keeps issuing more macros if IFOR is ~~not~~ asserted.

Need micro code control to select IF into OF. Add PROM bit.

OLD

RAM OF SEL
PROM OF SEL

DIAG	RAM OF SEL	PROM OF SEL	
0	0	x	RETURN DATA
0	1	x	SR
1	x		UW, UA

NEW

DIAG	OF SEL	PROM OF SEL	
0	0	x	RETURN DATA
0	1	x	SR
1	0		UW, UA
1	1	x	IF

] may want to expand this to include diag read of RAM & SR

Natsemi

DS1650/DS3650 TS MC3450
1652/ 3652 OC 3452

TI 75172
174

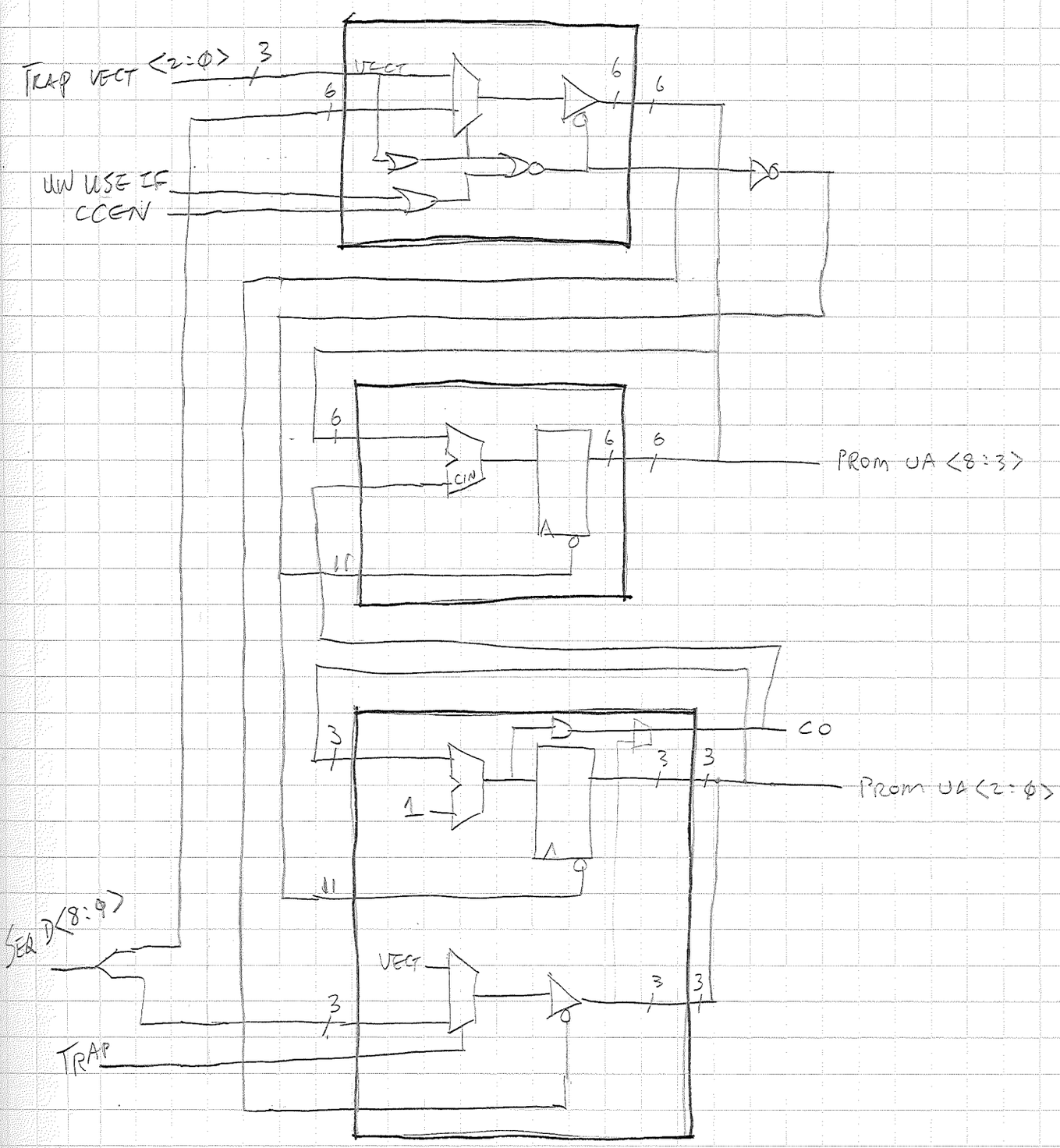
TRAP

UUN

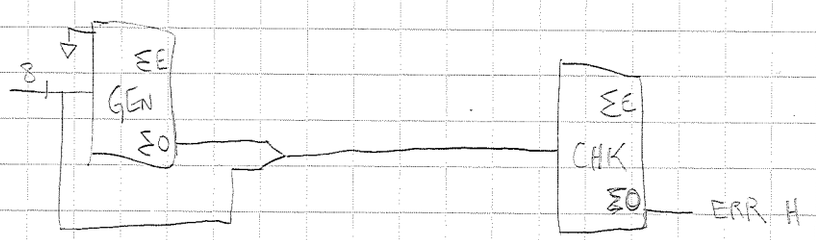
SEQ D<8

TRI

Replace 2910 & trap logic with PALs



check for IF empty via Bx.



Augat:

Wire Wrap

1 wk data entry from netlist
<1 wk wrap.
10¢/wire
$200 programming

Symbolics

X8136-SCH131-2TG

5-9 $1746
10-24 $1358

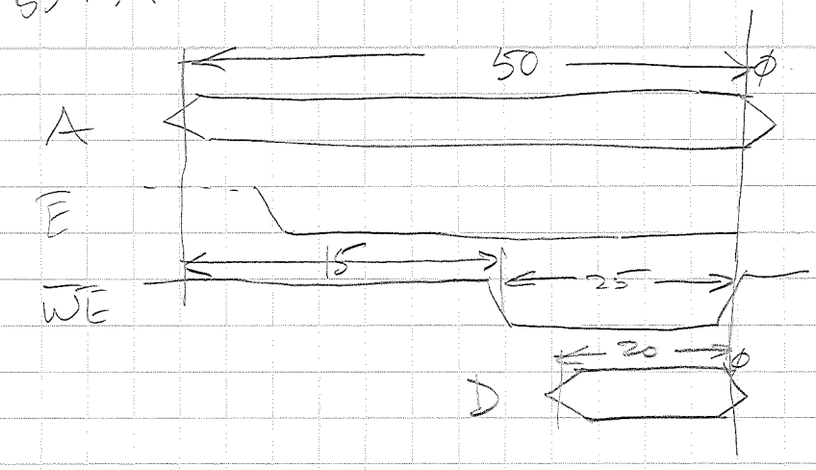
3 wks.

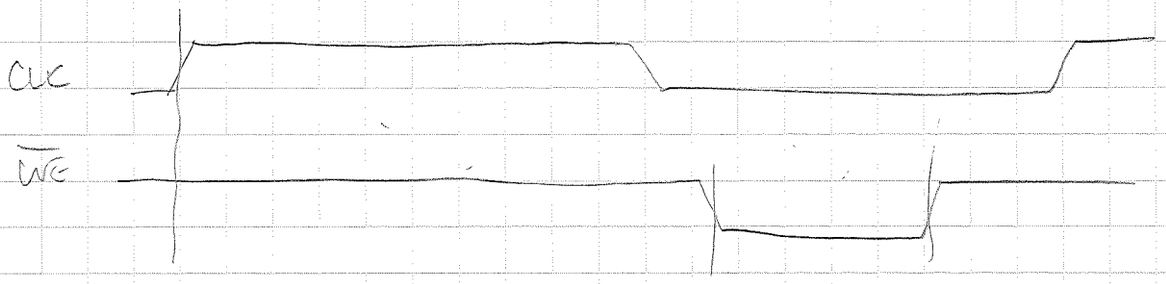
Paddleboard ?

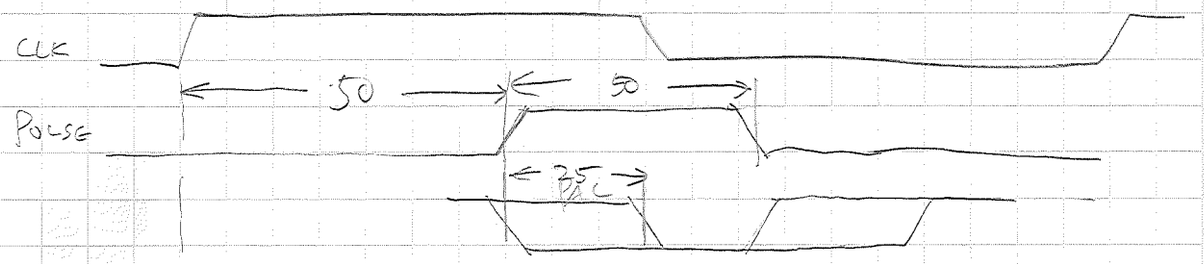
Schematics

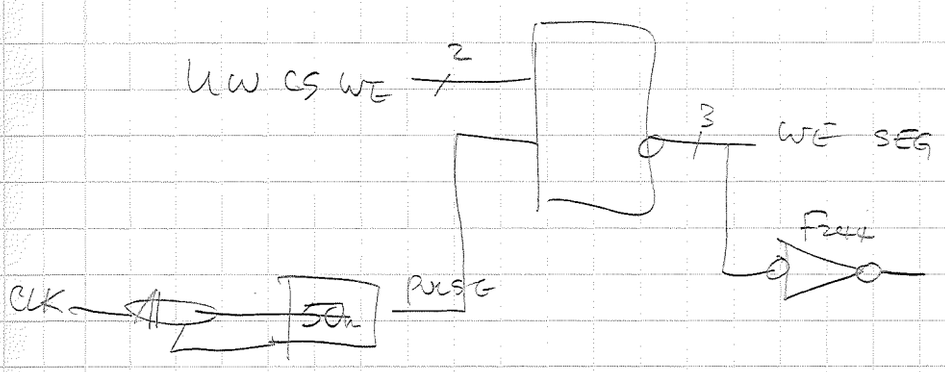
CLK

55 ns part

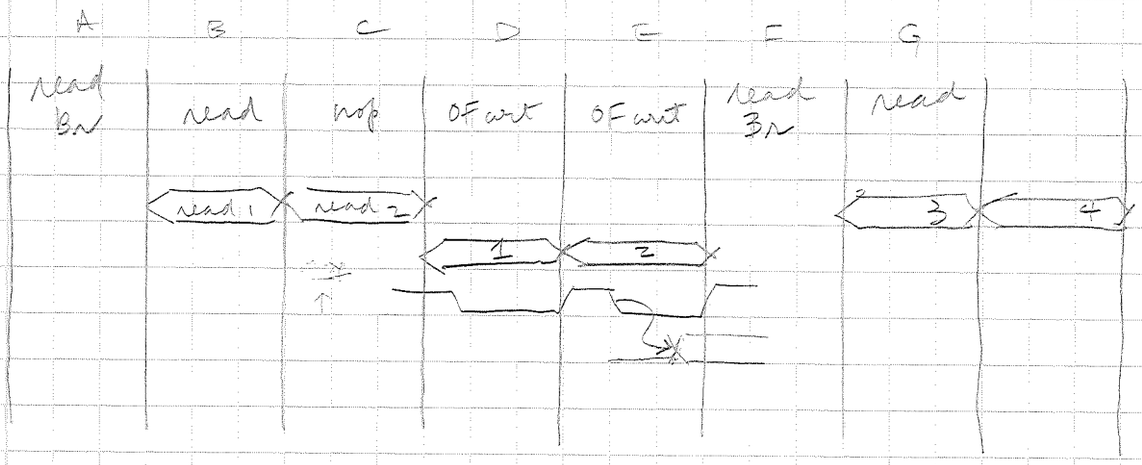

50
A
E
15
25
WE
20
D


CLK
WE

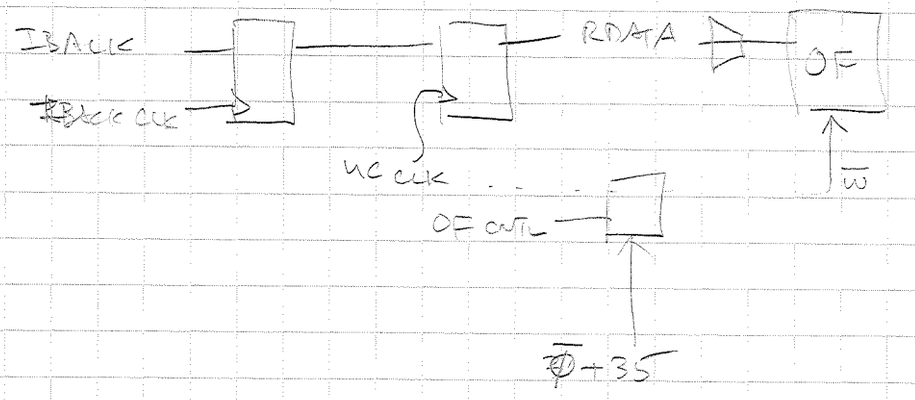

CLK
50
50
PULSE
25

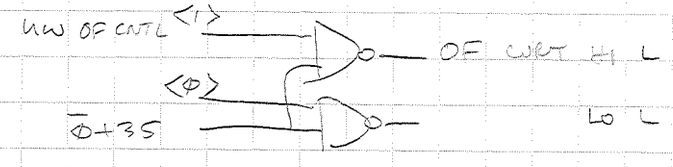

UW CS WE
2
3
WE SEG
Fast
CLK
50n
PULSE

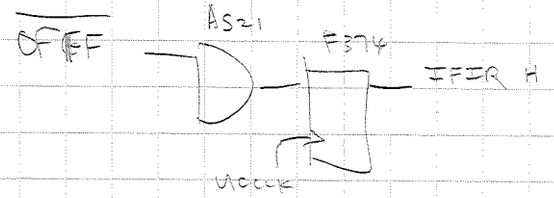
How does memory read work?

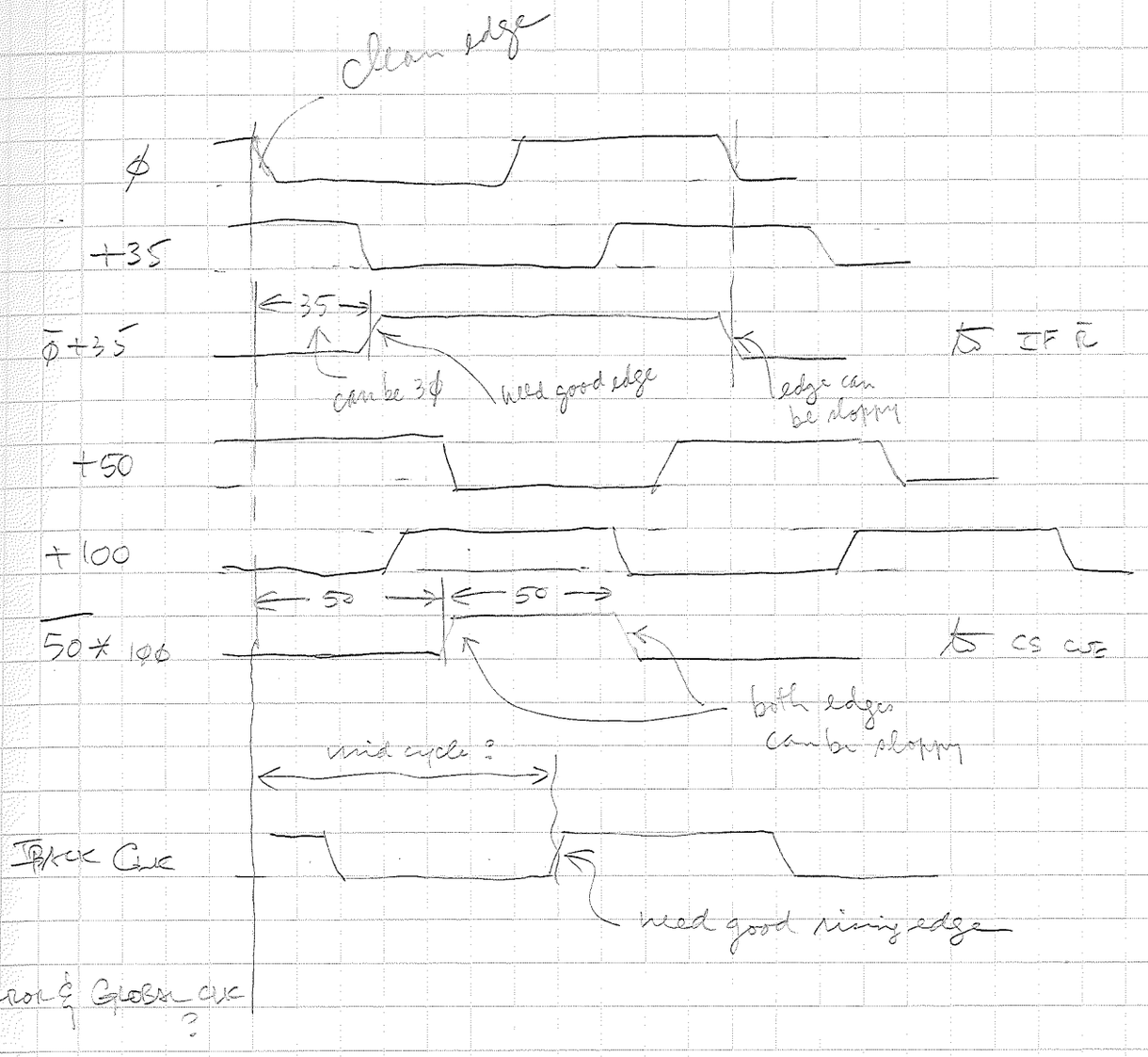


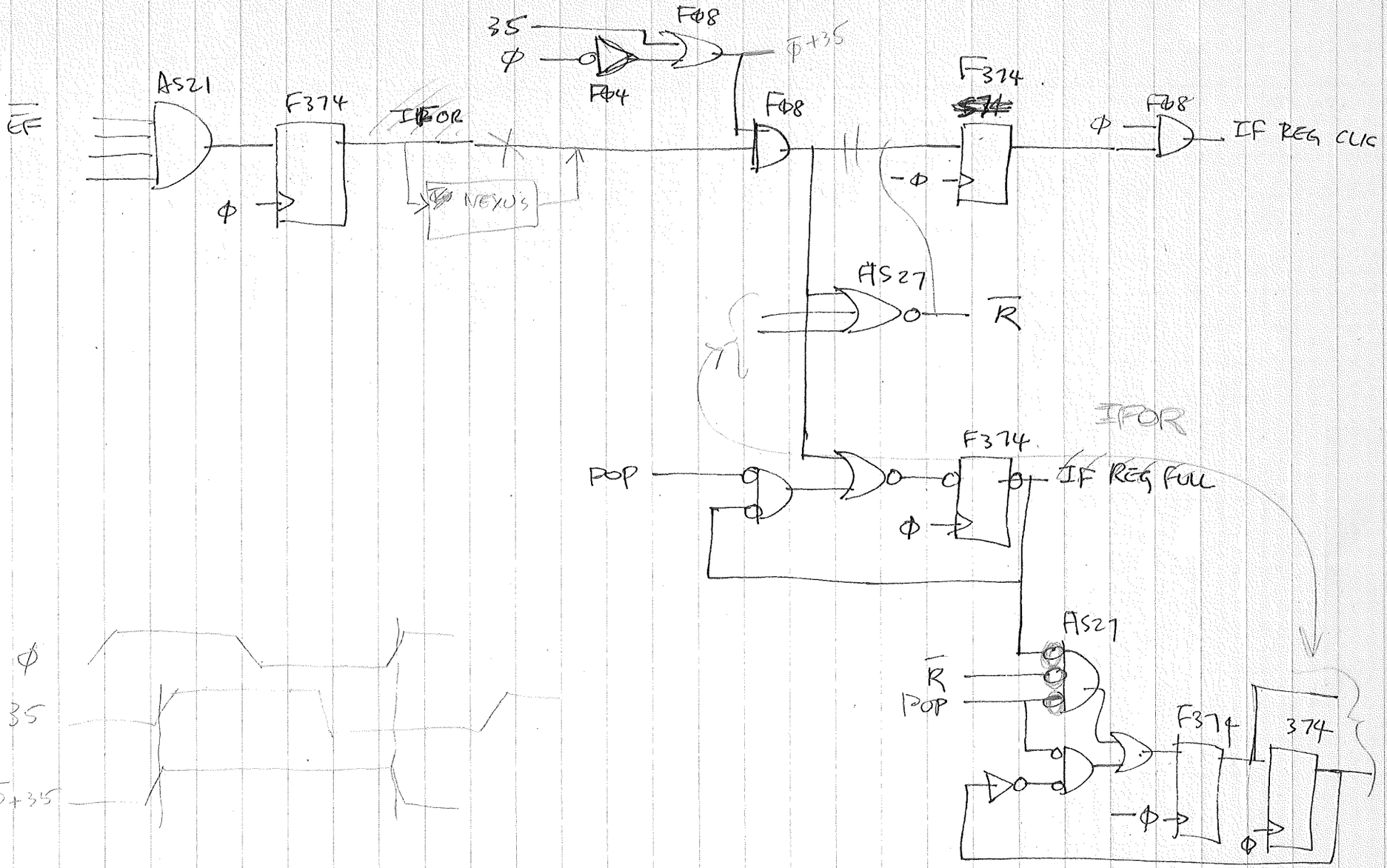
1. Assume Inst is clocked in array board during cycle B.
2. Assume data is valid during cycle C.

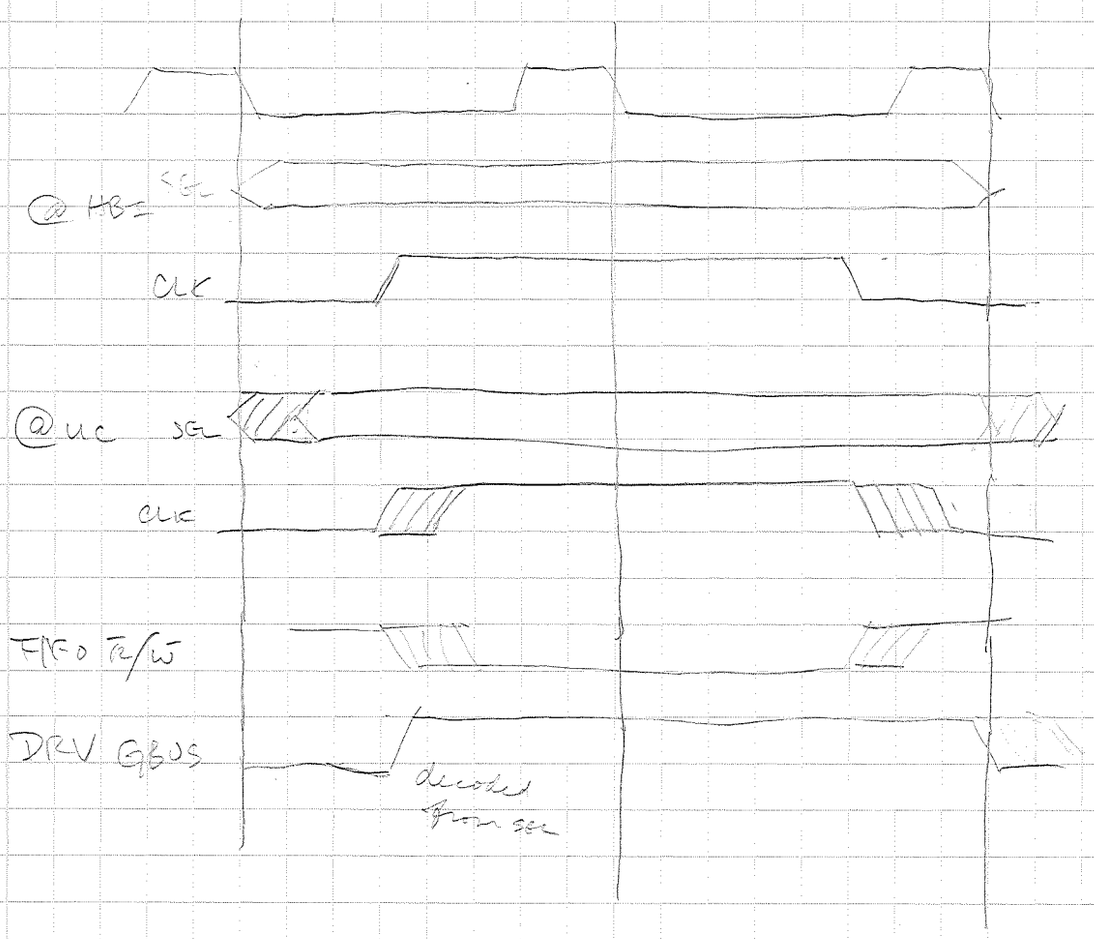


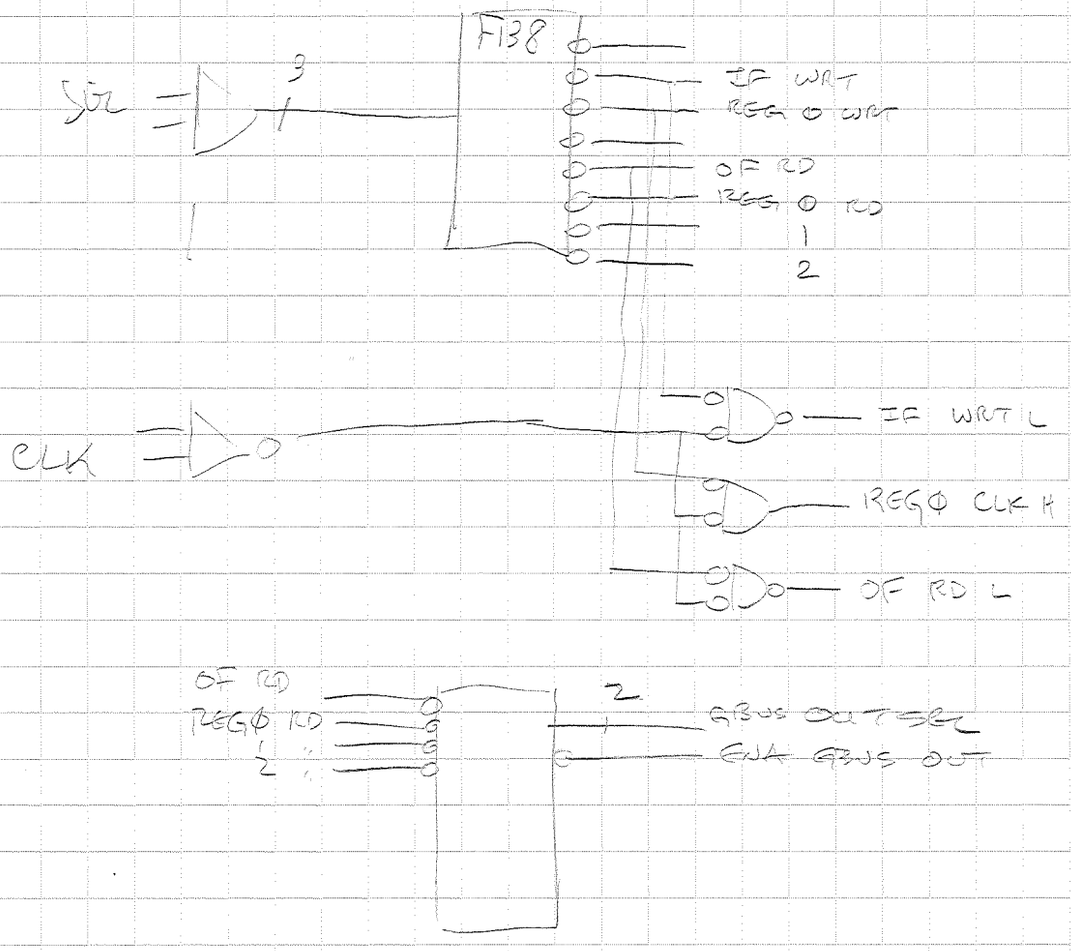


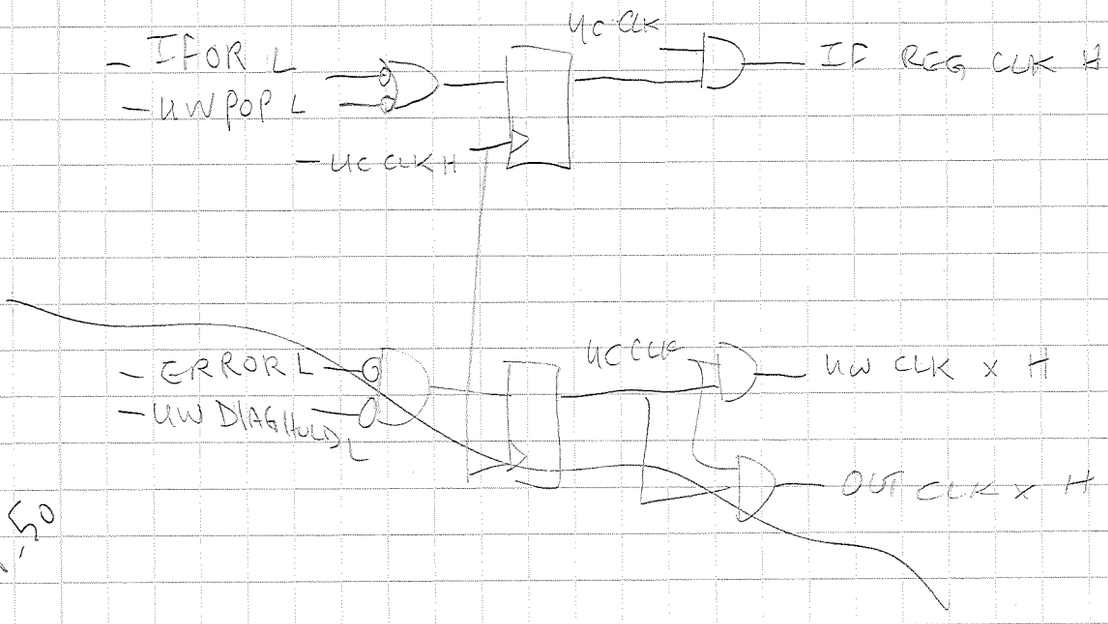



clean edge
ϕ
+35
ϕ+35
35
can be 3ϕ
need good edge
edge can be sloppy
+50
+100
50
50
50 * 100
both edges can be sloppy
mid cycle ?
Track Clk
need good timing edge
Error & Global Clk ?

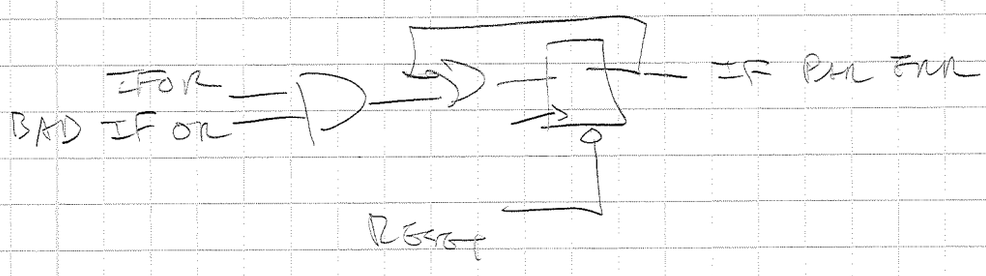

35
Φ
F04
F08
$\overline{\Phi+35}$
AS21
F374
IFOR
NEXUS
F08
F374
Φ
F08
IF REG CLK
AS27
$\overline{R}$
IFOR
F374
POP
IF REG FULL
Φ
AS27
$\overline{R}$
POP
F374
374
Φ
Φ
Φ
35
$\overline{\Phi+35}$

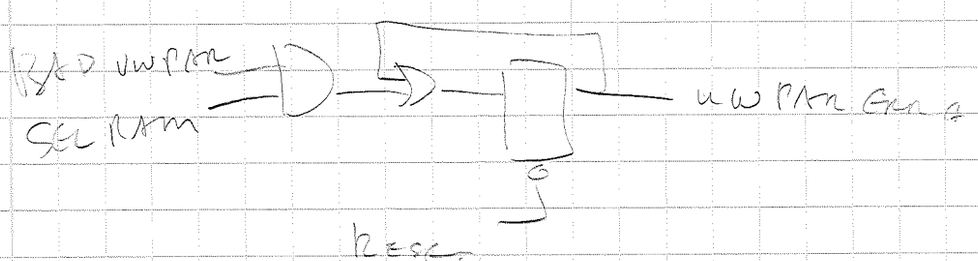

@ HB=
CLK
@ uC SGL
CLK
FIFO R/W
DRV GBUS
decoded from SGL


F138
IF WRT
REG Ø WRT
OF RD
REG Ø RD
1
2
SEL
CLK
IF WRT L
REGØ CLK H
OF RD L
OF RD
REGØ RD
1
2
2
GBUS OUT SEL
ENA GBUS OUT


- IFOR L
- UWPOP L
- UC CLK H
UC CLK
IF REG CLK H
- ERROR L
- UW DIAGHOLD L
UC CLK
UW CLK x H
OUT CLK x H

see 1,50


IFOR
BAD IF OR
IF PAR ERR
RESET


BAD UW PAR
SEL RAM
UW PAR GEN
RESET

25°C

	S	ALS	AS	F
00	5	11	4.5	
04	5	11	5	
153	18/9/15	21/15/18	12.5/8/11.5	
157	6/12/12	~~10/5/11~~	6/11/10.5	
182				
244	9/15	10/20	6.2/9	
257		12/22/18	6/11/9.5	
280				
299		19/22/22/		
374		16/18	9/10	
253		21/14/16	13.5/8/12.5	

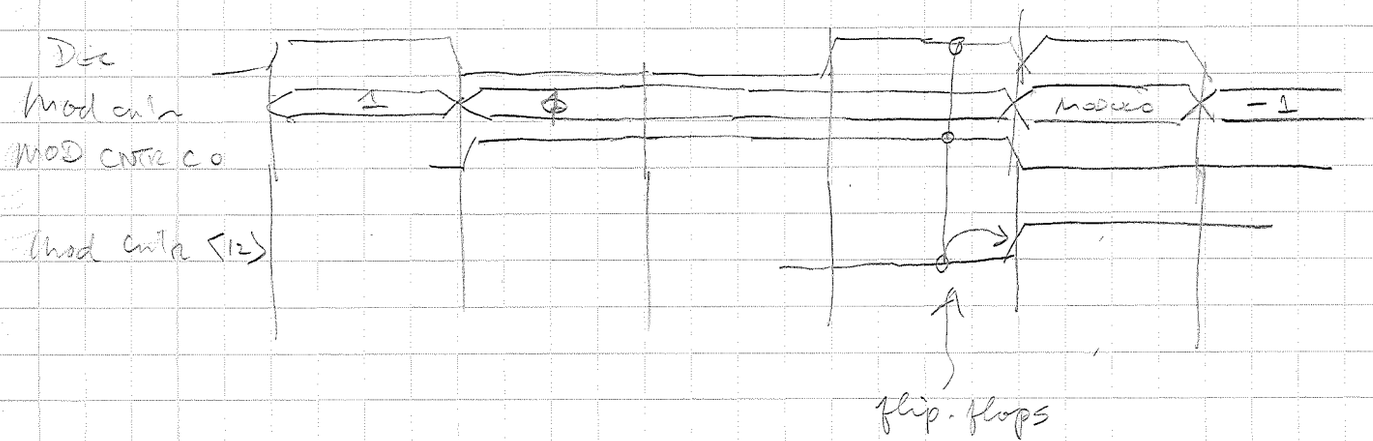
	sheet	IC	HM	Xreb
CMSET	~40	345	~2MB	1.7M
~~UCSET~~ UCSET	~20	318	~1MB	.7M
UCFLAT	~20		~2MB	.5M
UCFLMT2			.6MB	

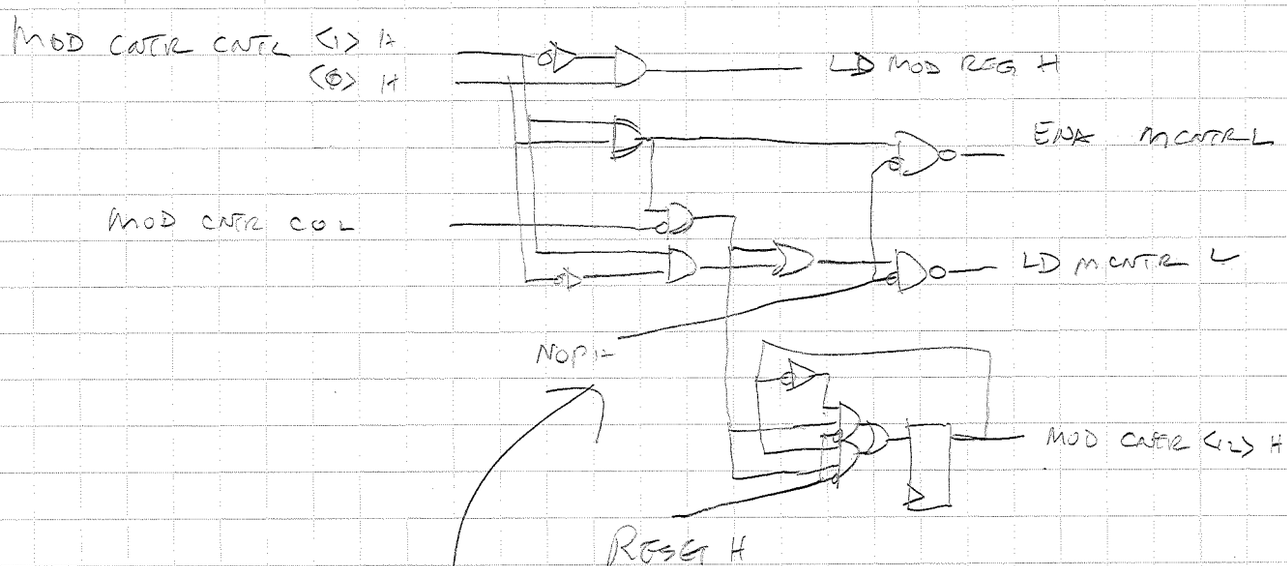
8/13

IDT 16K x 4

1st Silicon within ~~two~~ days, sampling in couple weeks
Now expensive than module.
break even in 1 year.

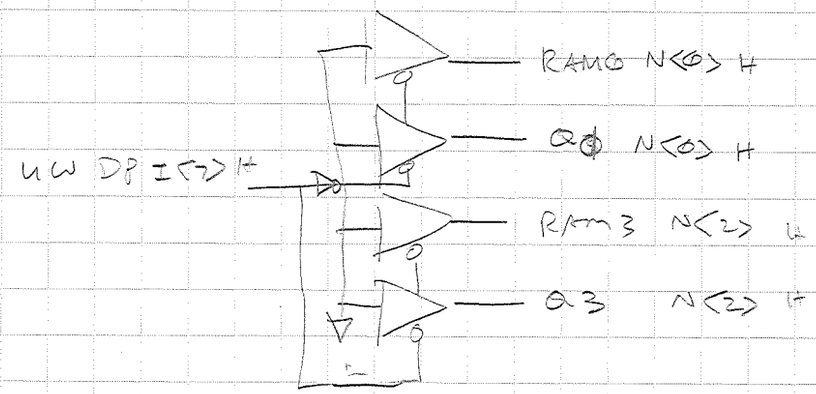
Price decrease since Sept $295 in 100 QTY 55 ns





<1>	<0>	
0	0	HOLD
0	1	LD R
1	0	LD C
1	1	DEC

No need, clk is NOP'd



4 addition ADDR bits

~~4 microcode bits~~

- 1 F257 mux
- 1/2 F244 (with mNAen bit)
- 1 2901
- 1/2 PAL
- 1 AMS569 } mod carry /
- 1/2 F374
- 1 F244 } output. only 4 expansion
- 12 I/O pins

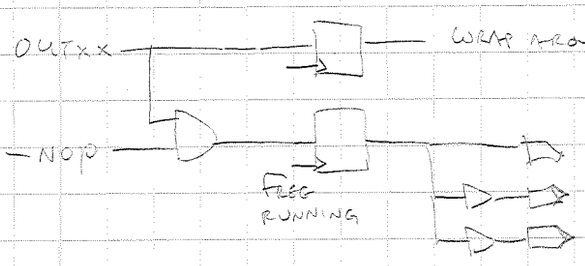
6 1/2 ICs 140 pin

~~1/2 F374~~ } ucode FF & parity check
~~1 F280~~

8

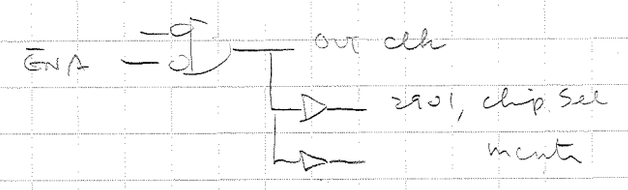
RST	ERR	DIAG	OUT NOP
X	1	X	1
X	X	1	1
1	X	X	1

OUT NOP no ops OP, ZIP LOC, WE, LATCH, SEND to be sent out.
CUBE ENA ? MEM BUF ENA ?



RST	ERR	DIAG	HOLD 'NOP'	2901	MCNTR RST	CHIP SEL RST	OUT REG
				CLKS			
1	X	X	X	X	X	X	X
X	1	X	X	ϕ	ϕ	ϕ	ϕ
X	X	1	X	ϕ	ϕ	ϕ	ϕ
X	X	X	1	ϕ	ϕ	ϕ	ϕ

MCNTR & CHIP SEL clks need no critical relationship to 2901 & OUT clks
OUT clk likes to be 'inform' 2901 clk. to get some 2901 hold time

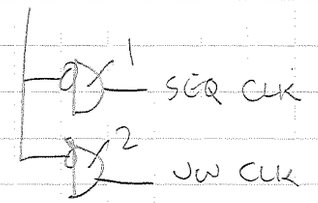


AS02	1 - 4.5
F02	2 - 6.5
F374	4 - 10, $t_h = 2$ $t_{su} = 2$

2901 $t_h = 2$
2910 $t_h = \phi$

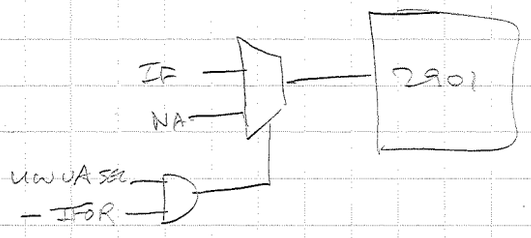
2901 clk in front of (or same as) UW REG clk

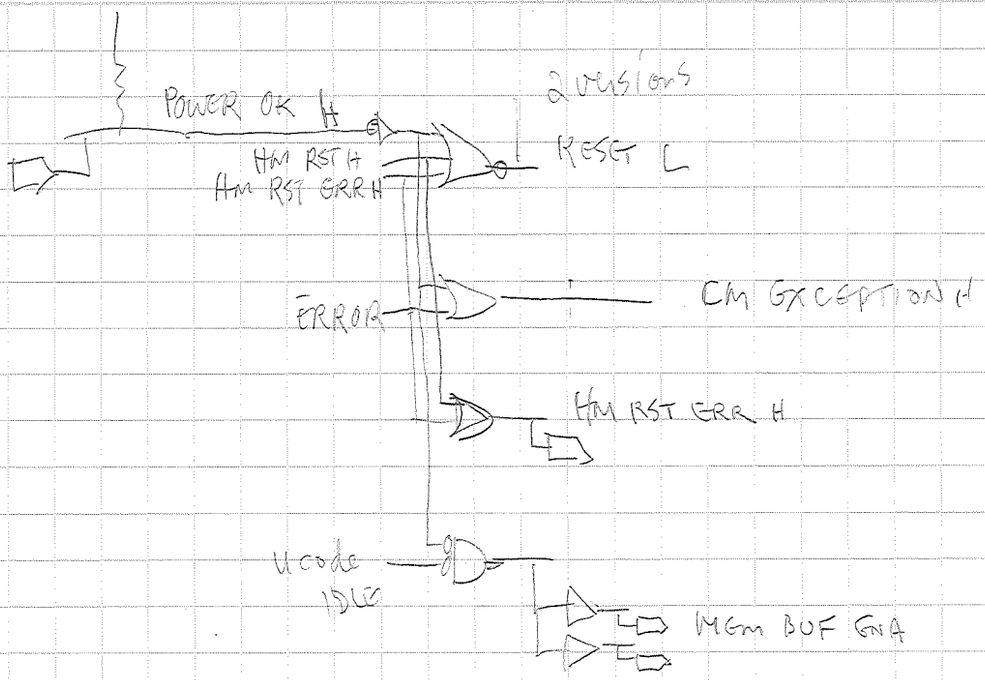
2910 clk " " UW Reg clk

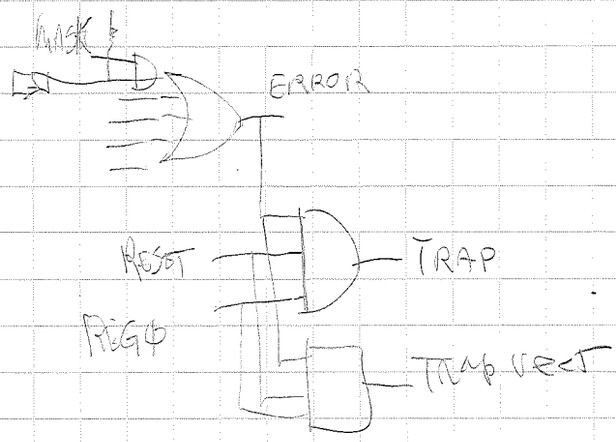


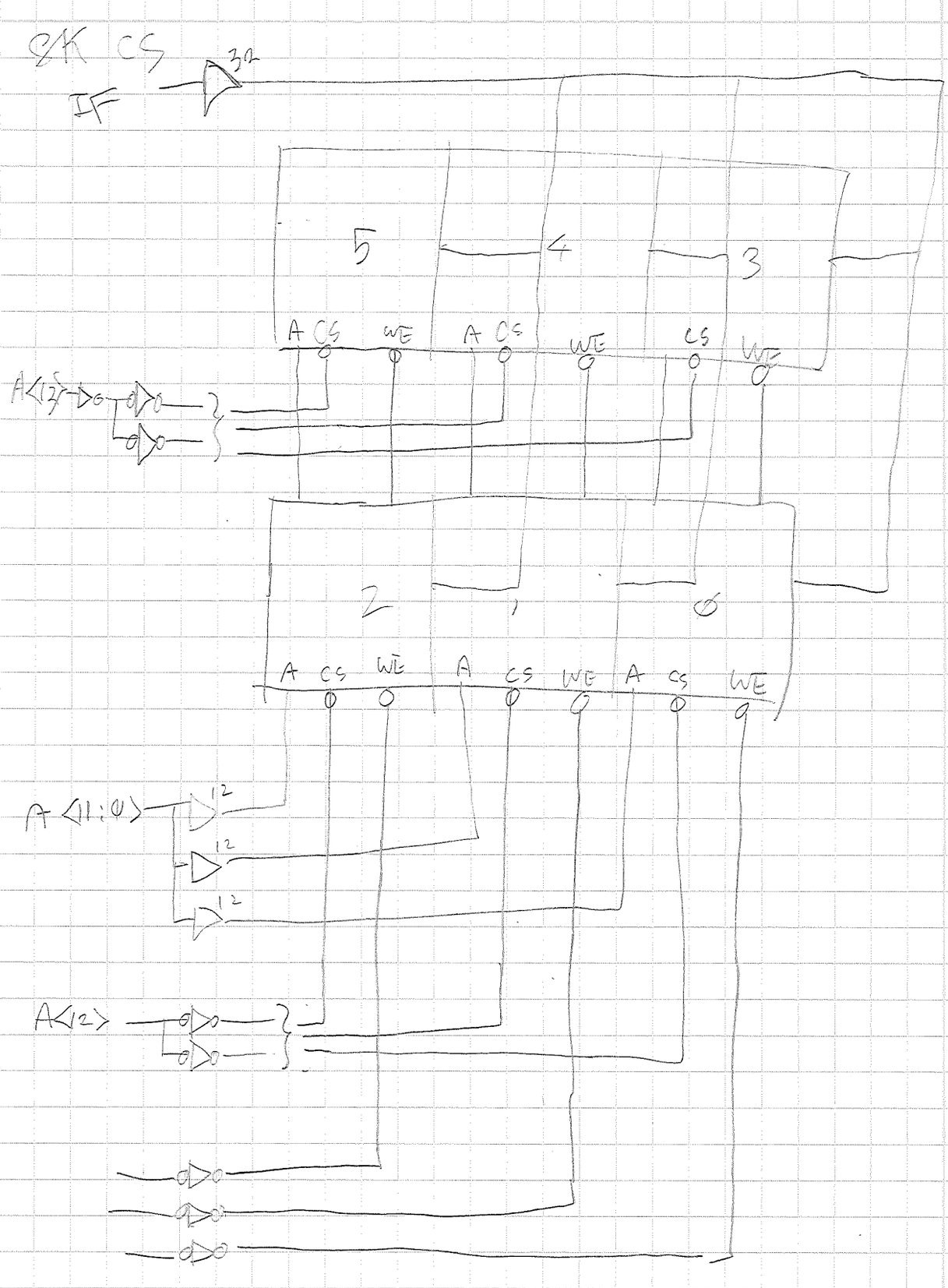
SEQ CLK can be free running (eprom must be)

ERR	DIAG HOLD	UW CLK
X	1	ϕ
1	X	ϕ




POWER OK H
2 versions
HM RST H
HM RST ERR H
RESET L
ERROR
CM EXCEPTION H
HM RST ERR H
Ucode IDLE
MEM BUF ENA

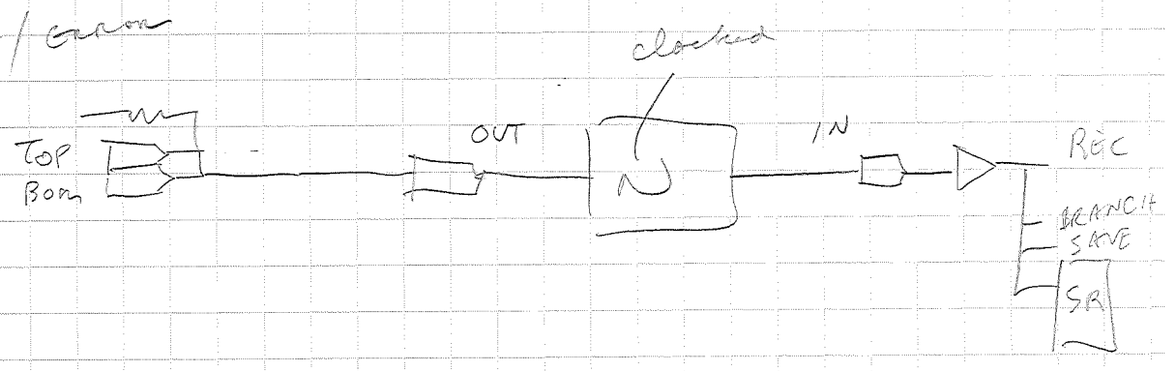

MASK L
ERROR
RESET
TRAP
PEG4
TRAP VECT


CK CS
IF
32
5
4
3
A CS WE A CS WE CS WE
A<13:5>
2
1
0
A CS WE A CS WE A CS WE
A<11:0>
12
12
12
36
/
A2
A<12>
4
6
/
10

MCRT CNTL
<>

With clk inhibited by NOP, CHIP SEL <> { ∧
need no qualifying thru PAL.

GLOBAL / CACHE



UC / MEMORY timing

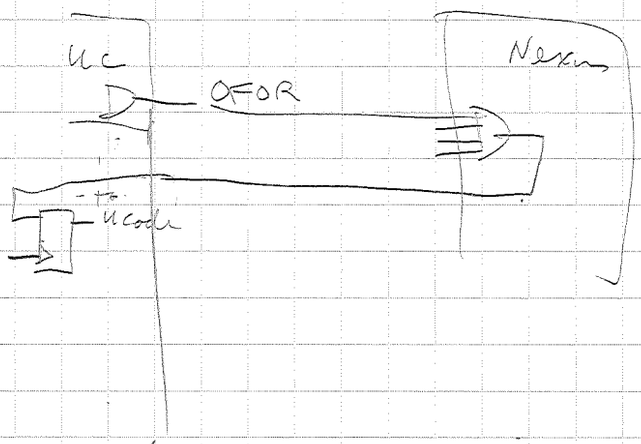
OUT CLK

SIGNAL	4/10	3	2/8	3	2-8 ?	2	2	24 - 3φ
	F374	CABLE @ 2ns/ft	F244	BP @ 2ns/ft	trace @ 2ns/in 6"/bd × 8 = 48"	input cap @ 5pf per TTL × 8 = 40pf @ .05ns/pf	F374 T_{su}	

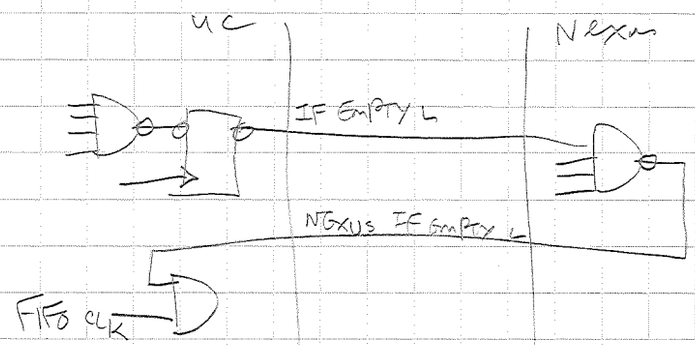
IF delay line works with rising edge then invert!

OFIR is now useless, since mode is going to assume an empty OF before block (512 LWD) transfer.

Instead OFOR is an indicator to uCode that OF is empty. Nexus connection should be



IFOR / Nexus connection



delay from clock edge to input AND GATE (FFRD) should be less than 30 ns. Currently IF EMPTY is generated inside PAC, may need to move it out.

Ø
16
31
31 + SAVED
SAVED

IFB 291Ø — OP, ITERATION CNT
MCNTR
CHIPSEL
<Ø> LAST

IFA 2911 — MADDR
WDATA
ARG INSTR

1. All dips bot justified to pin 1.
2. 'GND L' signal, separate to per IC.
3. Wiring color — RED VCC
   BLK GND
   YEL OTHERS
4. Wire up filter caps for each IC.
5. 'NC' signal means no connection
6. see list for additional no connection signals.
7. Wire all even pins on connectors J11, J12, & J16 to gnd.
8. indicator for each pin 1 on pin side.

1. Placement by Friday

2. Bd possibly by Next Friday

No color coding.

Paul Dever to call.

Need geometry of PG312

-8136 - UG300 4 available. finished

308 & 312 2 each available w/o pins.

1. ANSI Tape
2. ~~print from~~ VMS
3. ~~data~~ I/O

ANSITAR on VAX

DATA I/O

tip DATA I/O

download

~>(filename) ↵

upload

~<(filename) ↵

disconnect

~.

60

	From	To	
	IBACK <16:0>		17
	GLOBAL		1
	ERROR		1
—	FIFO RDY		1
—	FGYNBUS GNT		1
—	SAFETY PIN		1
		INSTR <16:0>	17
		OP <2:0>	3
		CHIPSEL <11:0>	12
		MADDR <15:0>	16
		AFLIP <3:0>	4
		SENSR	2
		LATCHR	2
		FDIR	1
		SCAN	1
		RGAD	1
		MEMBUF GNA	1
		CUBE GNA	2
		WE HI LO	2
		CLK	2
—		PULLUP	1
		GNA LED	1
		HM RST	1
—		ZIP LOC	1
—		FIFO STRNG	1

71

93

UCPROTO

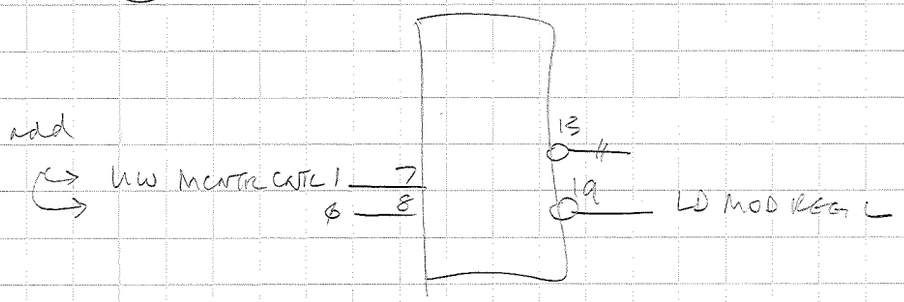
(1) Flag out gets ~~CWDATA~~ CWDATA FLIP <3:0>
IFLIP out gets " <15:12>

(2) Change IFIR H to IFIR L to NGXUS
change NGXUS of FUNC L to H
Change OF FUNC L to H.

(3) change CHK RDATA W<1:0> from negative bits to wrong bits

(4) ~~MASKERROR~~ REG MASK ERROR → REG MASK ERR
RESET ERROR → RESET ERR

(5) MREGLO PAL



(6) Add NWALU0 to ALUM PAL

(7) add REG ERR H to BR PAL

(8) Wire OR CCA12 & CCB19 of BR PAL

(9) add ~~SELRAM~~ SELRAM L to OF PAL

(10) change SEQLSB PAL to 16R4, add FOE for CO

(11) Swap pins 18/19 on PROM HI PAL

1. drill hole cleaning in custom boards
2. HBI, Nexus priority
3. extend

SAVE every.
DONOT compile

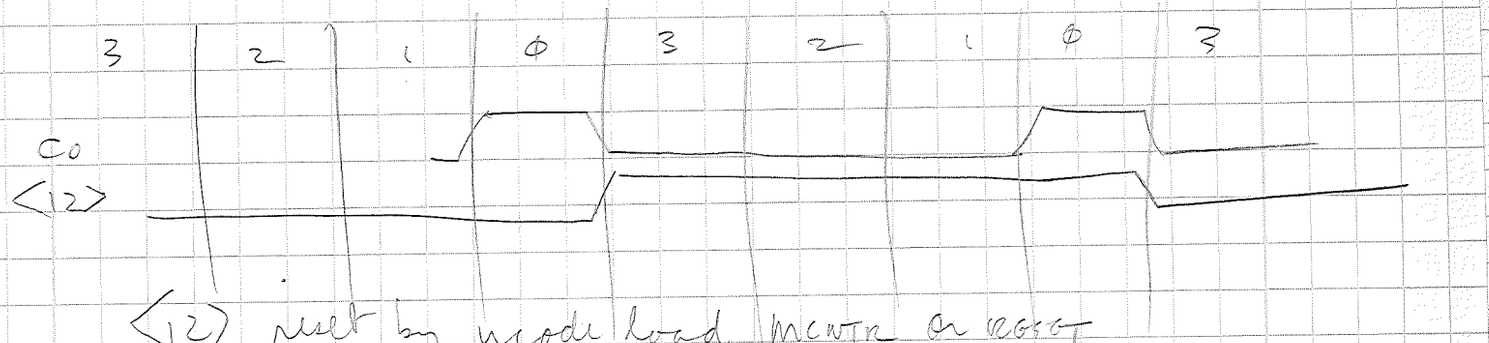
USE STABLE FILE ON

cnet, cnet

DIFF file file

Change in graphics
Compile
Plot

Mod cntr operation



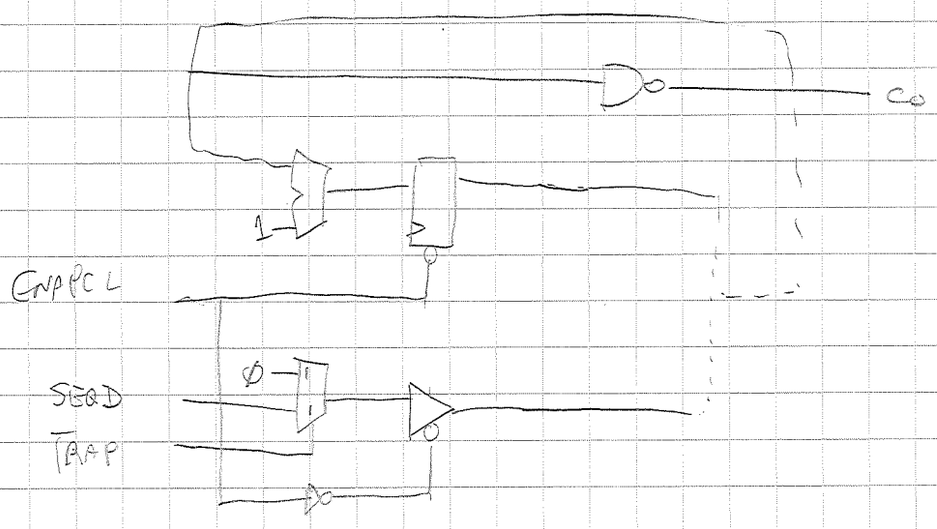
<12> set by ucode load MCNTR or RSET

12/13 Also: Branch on MCCO works in one way only:

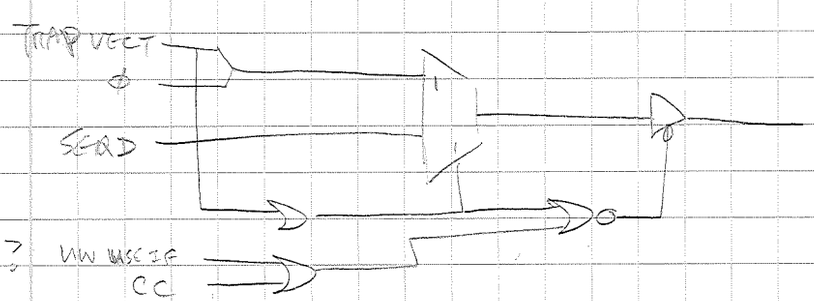
X:/ DEC mod cntr, Br MCCO ; MCCO = 1 iff mod cntr = 0 prior to this inst.

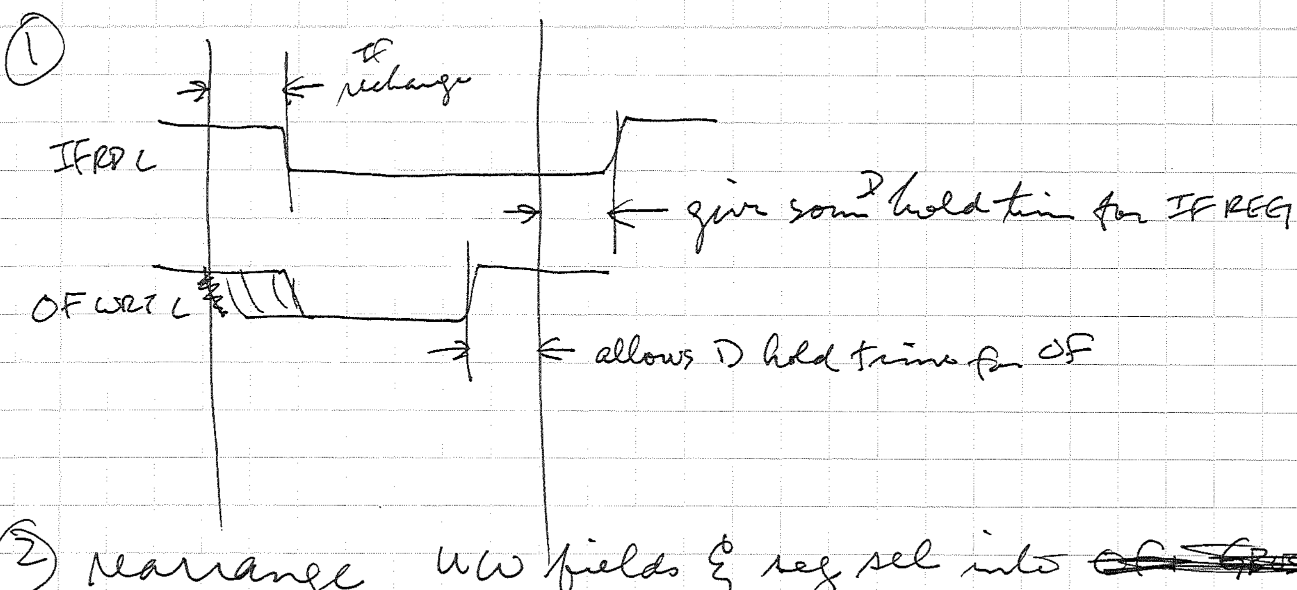
Inside ALU569 CO = down count * Tena * cntr = 0

PROM L6 See P. 37



PROM +1 I



① 

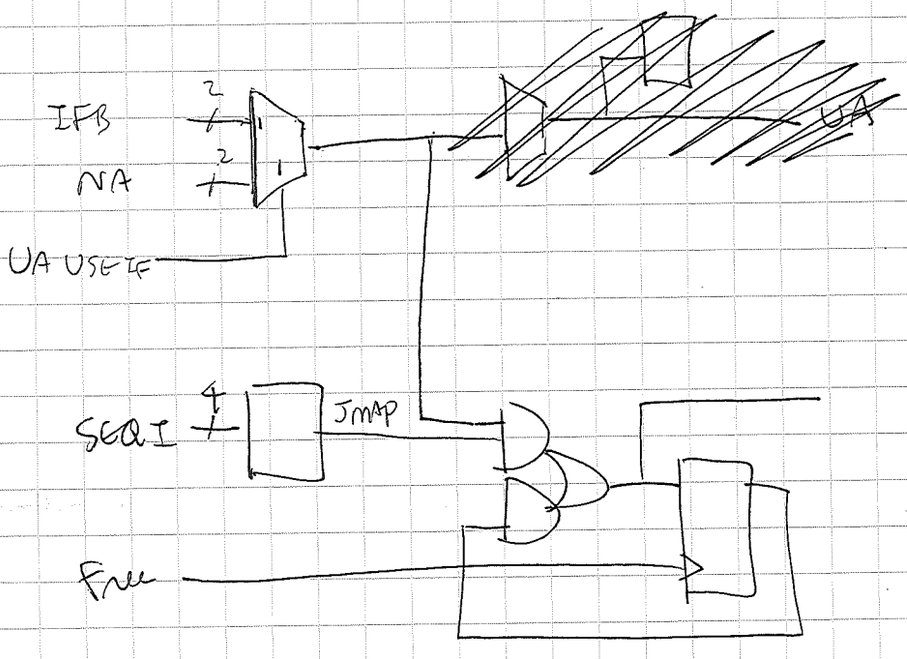
✓ ② rearrange uw fields & reg sel into ~~OF GBUS~~ OF-IN.

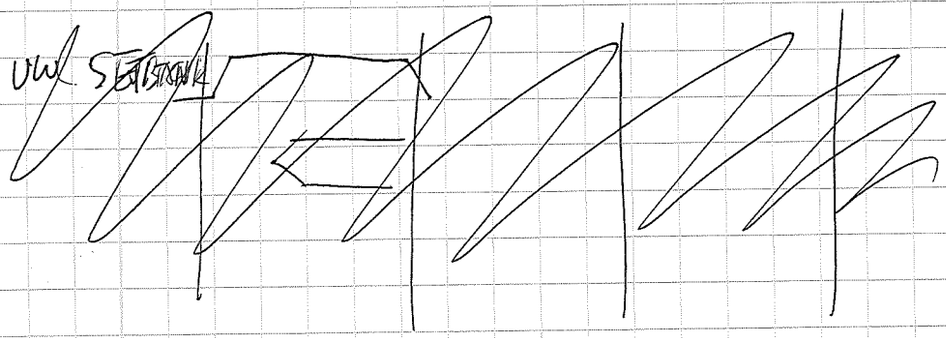
✓ ③ Add Madd <15:12> to REG 1.

④ fix CS ere? ease;

✓ ①. Add 2901 ~~ww~~ MADDR back to IFA & IFB
✓ ② fix IFB (2) input.
✓ ③ fix SR
✓ ④ fix mem qtr. [QTR] ✓
✓ ⑤ fix UW bits arrangement into OF IN, add madd <15:12> in REG Ø
✓ ⑥ add GBUS/NEX termination.
✓ ⑦ fix Nex flag? add syst err, OF FULL: [IF] ✓ [BR] ✓
✓ ⑧ fix SEQ CLK: [CLK] ✓
✓ ⑨ LSB → MSB 2910 [CI] ✓ [BANK] ✓
✓ ⑩ add diag hold FF bit into REG Ø [NOP] ✓
✓ ⑪ get rid of ~~RLD~~
✓ ⑫ get rid of LAST, DONE [BOOT]
✓ ⑬ fix branch code. [BR] ✓
✓ ⑭ mod counter 16 or 12? [ACCO] ✓, [DCD] ✓
✓ ⑮ add ADDR IN <15:12>
✓ ⑯ Add 2901 <15:12>, fix shift, zero
✓ ⑰ Add 2901 CO [BR] ✓
✓ ⑱ fix RDATA from 2BP
✓ ⑲ edge connectance.
✓ ⑳ add ~~RADR~~ RDATA wraparound, ~~[RDATA]~~ IBACK

✓ ㉑ add mem buffer ena [~~NOP~~] ✓ RST
✓ ㉒ fix uw cont check.
✓ ㉓ WE = 3 [DCD] ✓

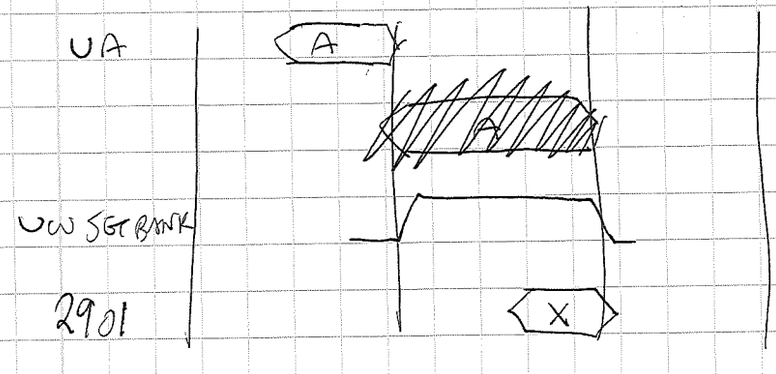




A = SEQ BANK = X

XB :

don't work

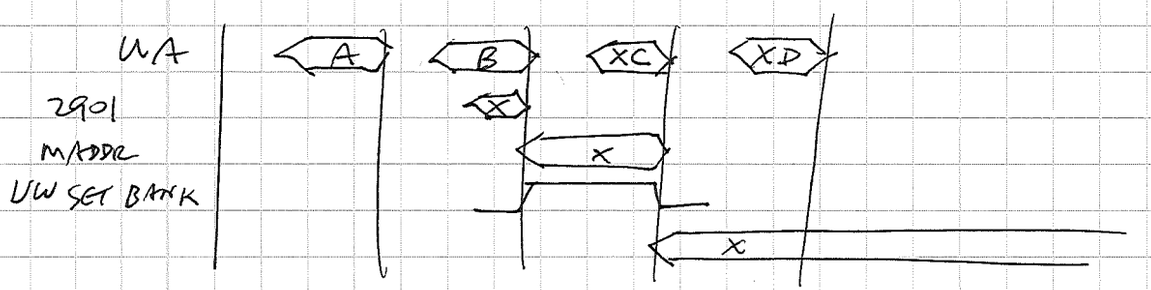


A : set up 2901 = X , x = next bank

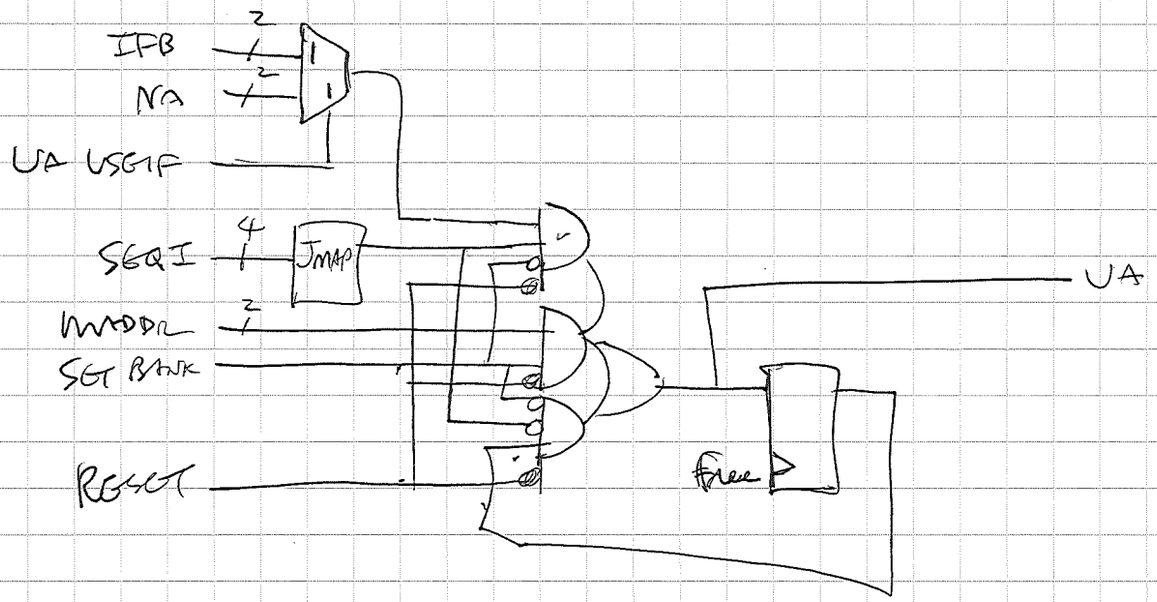
B : set BANK

XC :

XD :



13



18

- ✓ 1. fix chip sel dly
- ✓ 2. add chip sel dly bit mux IBlock <9>
- ✓ 3. fix NOX connection version
- ✓ 4. add term to all receiving reg
- ✓ 5. bring out WA
- ✓ 6. check on OFIR polarity
- ✓ 7. get rid of OWIFLIP [IFLIP1, 2]
- ✓ 8. fix OUTCLK add A version
- ✓ 9. fix clk mux RSP8 instead of F244

12/6

AMD 29116 1-100 95
101-1000 50-60

29117 sampling Jan '85 — 116 with F/O separated

29116A " "
25% + performance

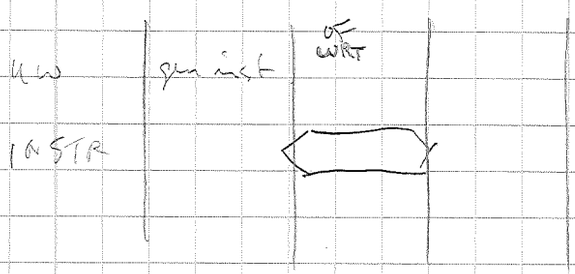
29L116 half power

PAL 35 ns in production
25 ns in April.

HDC 9580 Samples in April
9581 "

A: gen INST

B: WAIT OF [illegible] INST



placement generation

(loader "A:>clem>dump-file")

(dump-clem-file) g://u//c. - - -

Sending files over phone line to Angat

tip angat

~(Set) echocheck

~> filename

THINKING MACHINES

; phone down

INTEL

John Hyslop application engr.

12/12

PG 3.12 COST

ALUHI.1	
ALULO.1	
ALUM.1	
BOOT.1	
BR.1	BR.2
CLK.3	CLK.4
DCD.1	DCD.2
ERR.1	
FLAG.1	
FLIPPER.1	
GBUS.2	
IF.2	IF.3
IFLIP.1	
MCCO.1	MCCO.2
MRHI.1	
MRLO.1	
NOP.3	NOP.4
OF.2	
OP.2	
PROMHI.X3	
PROMLO.1	
PROMPC.1	
QTR.1	QTR.2
RDATA.2	
REGΦ.1	
RST.2	RST.3
SEQD.2	
SEQLSB.1	
TRAP.X2	

12/12 AUGAT

$.25/sq in/layer (mass production) PCB

Unibay test system up to 14 x 14 — 1. need custom test jig
2. or tested outside

$150 bare board
400 wiring

Impedance ~65Ω

Ø profile sockets for component insertion.
Not machine insertable.
Can wave solder if no wire on solder side.
Repair - equivalent to multi-layer, solder-removable dangerous.

> C:>D
A:> potato > support > compile-exp.lisp

t, nil - constants
true & false

(login 'clem)

<select> E

^X ^F A:>bradley>potato-chip>tran>compile
compile-exp.lisp

M-X C-B ↵ — compiles buffer.

M-. clem1 ↵

create your fun in the editor

M-X C-spam B ↵

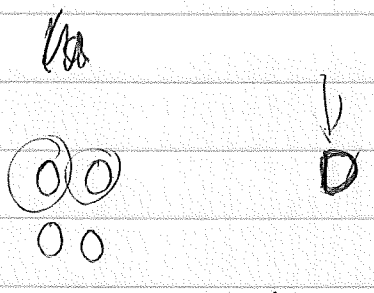
move to ins
M-X Byte EV_into_buffer
(FLIP) and key
any key to return.

<suspend>
function name

(grind-top-level (*) space
{as many times as possible on 1 st line}

M-X Write Region
q:/u/clem...
SUPER-L

(A * B) (* A * B)



>bradley>p-c>obs>sim>comp.1

Rev 7.0

/U0/LIB/MASTER.LIB
/U0/SCALD/MASTER.LIB
} change both

in drawing directory see /u1/tmc/schem/cmboard

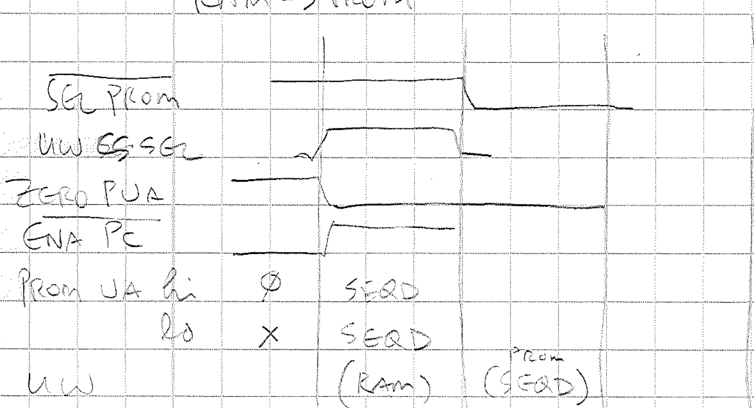
SCALD.CMD

```
Output ..... list;
Library-file      ;
  .
  .
  .
end.
```

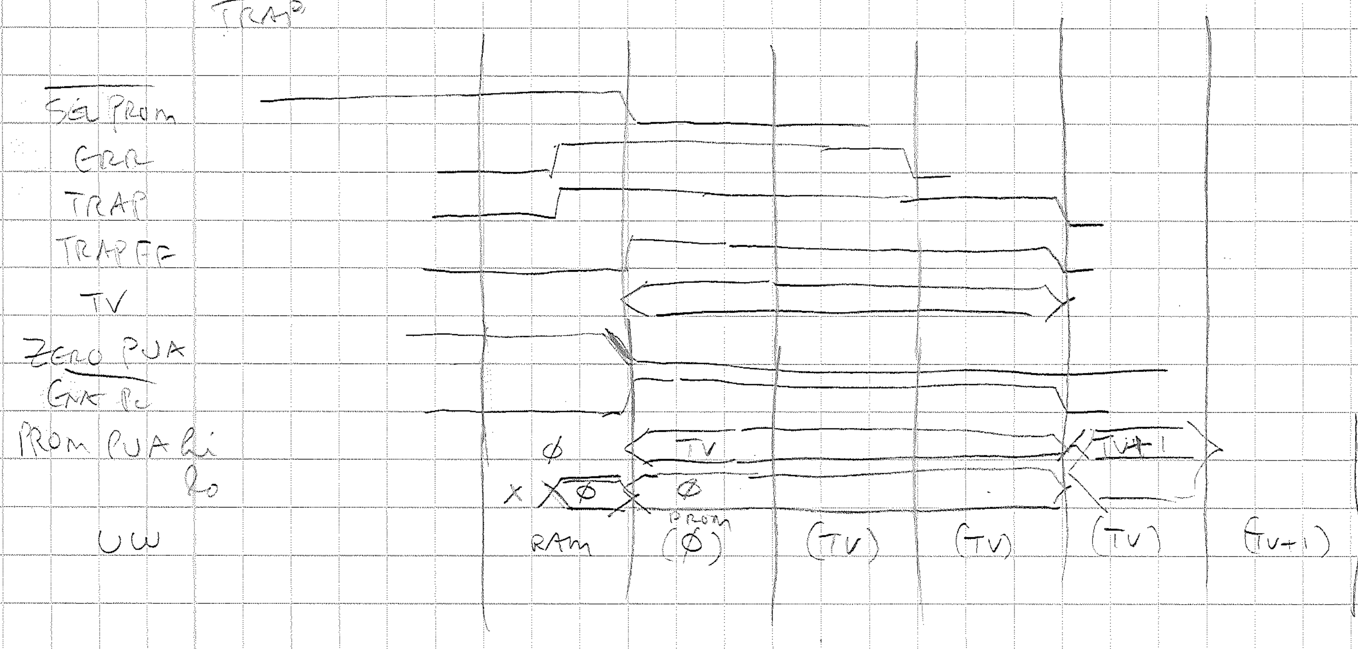
CUST3

1. Switch & add saved IF SEL IF
2. Latch Error [IBACK] ✓
3. Connection
4. trap a). MASK trap problem } [CI] [trap] ✓
   b). OF CNTL switch problem } [PROMLO] [PROMHI]
5. Pullup MASK TRAP, invert polarity.
6. Swap maddr 12, 13 with 0, 1 @ EBANK
7. use OF RD for mem qtr switch [QTR] ✓
8. add RESET C [RST] ✓

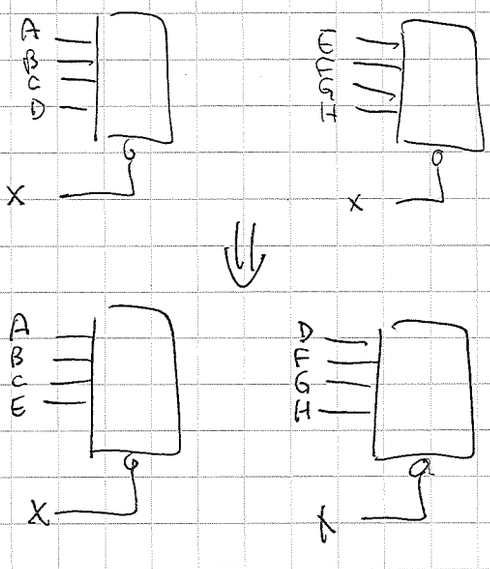
RAM → PROM



TRAP



1. feedback



2. bi-directional ~~sign~~ recognition

3. Change of feature.

Q. Property sec II
TERM

Rev 7.25 by March.

UC / NEX

1. No need to send exception to NEXUS, NEXUS will ask NEX comp GDR to HBT an exception

2. clock OFOR prior binding it to NEX, NEX OF entry may or may not be clocked at UC

Priam

11/24

Micropolis

100 qty	1304	$1435	2440 list
	1303	$1200	2140
	1302	$1170	1995

ESDI Q3 Q4 volume.

175MB drive

	1320	$1700	3035
	85m		

Richard Hodgson Micropolis Tech person

Interscomp. Apollo. Computervision

CDC

'86

3.3 GB each, 128 MHz

~3K / 370 MB drive
12K box controller
} 50 K Sabre system

Interim:

25 >1000 86 mB 5¼" ESDI drive shipped for 1 yr.

via Emulex SCSI board. ~500

↑
Roger Evans

2/8 MOSAIC

8MB memory.

100 ns cycle 40 multiplexed 32 bit.
dual rail, one write, one read.
access - up to 4 word/req.

AMD 29116 - graphics processor.

1024 x 1024	32	B/W
512 x 640	4,8	color b
1024 x 1280	32	" hi — 6 months away.

12 x 16 bd size 70+ chips interface 2 busses.

2 amps max/bd +5

85 MB Vertex 5¼"

2/11 SCSI = X3.131

IPI Gary Robison @ DEC

Maxtor 380MB ESDI drive available Sept 85
408-942-1700

Advanced Storage Tech
408-224-8010

SCSI approval by April

Feb mini micro list of vendor.

ADAPTEC San Fran
ADAPTOR DATA SYST CAN
WESTERN DIGITAL
~~SMS~~
Standard Micro Syst. Daniel Iroski Calif.
Emulex
Data Technology
Advanced Information Syst. SMD

X3.91M SMD Spec. Gene Milligan (CDC)
405 324 3638

2/19 CDC

1. available end of year — 10 mbit
   - R/W circuit change
   - media ~~oxide~~ plated change
   - head ? ferrite unchanged

2. MTBF
   included correctable

2. Controller used

   ADAPTEC
   Western Digital

   not mountable to CURREN II

3. MTBF

   - 15K hrs. — recover-able errors

   10^{12} - excluding known bad blocks

4. Bad blocks - Spec.

<8b defects

track & error free

+ 4,5 defects detected by custom

1 { missing bit
2 { pick up bit
3 { Stiffer

extremely rare defects > 1, 2 bits

$D_1 \xleftrightarrow{>1} D_2$ } looks like burst.

ADAPTEC OTR 2

Bill Nimce

2/ CDC

1. Head switch trim = 15 μs ?

2. defect ≤ contamination, length defined.
   bigger drive multi-defects on single track is flagged
   14"

3. 10MB version : will check.

Gmurex

Maxtor - media problem
AST - ?
CDC - runs

availability issue — 5 mHz ?
10 mHz ?

Medalist is released.

ESDI difference - functional.

Wed 10

as of 2/1

200-300 ~~QUEST~~ QUEST II drives shipped

controller house

~~4 4G~~

Data Tech Comp

Emulex

~~X~~EBEC SMHE only

CEC customer eval unit

section pulses only.

~~SMH~~

Major options:

1. Step mode / serial — ~~all~~ serial implemented by all controllers

2. sector marking — sector ✓
address mark found ✓
byte clk ✗

3. Diagnostics different

SMD

Gene Milligan ~~3070~~ 405 324-3070

3/6

Emulex

Tested 4 drives

1. ~~Hitachi~~
2. Maxtor } 10 mHz, all died
3. AST
4. CDC — 5 mHz, OK

beta shipped with CDC

1. takes bad block list with a 'format with defect' command. written onto each track of cyl 0.
2. ~~Hard~~ # of spares per track is 1 sector defaulted. but can be something else? Yes, up to three.
3. spare track is on 2 innermost cylinders.
4. rd error

Herb Silverman - ~~product~~ Engr manager.

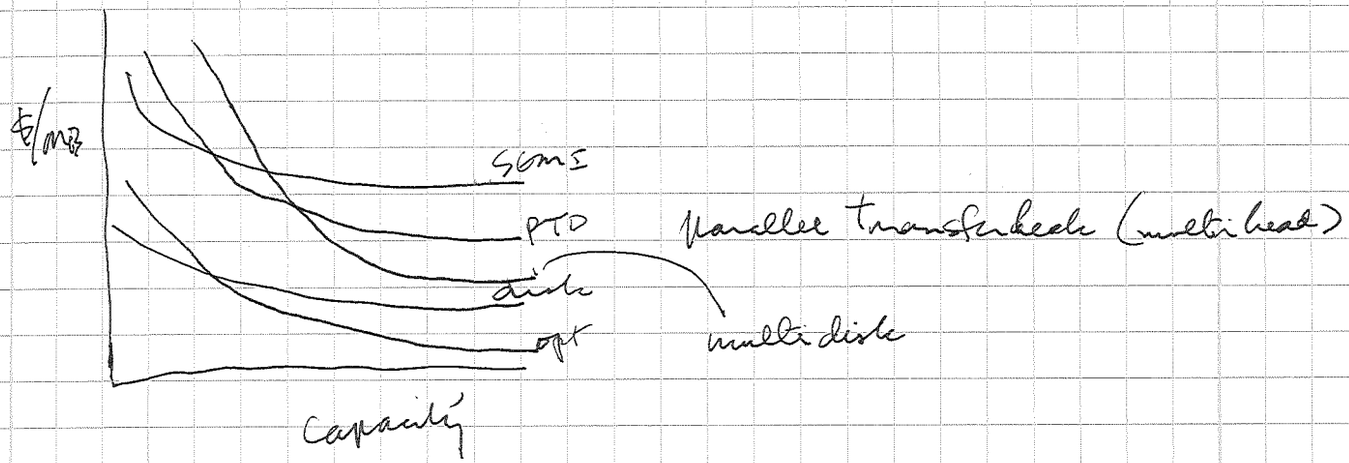
Intel multibus I → SCSI, dumb

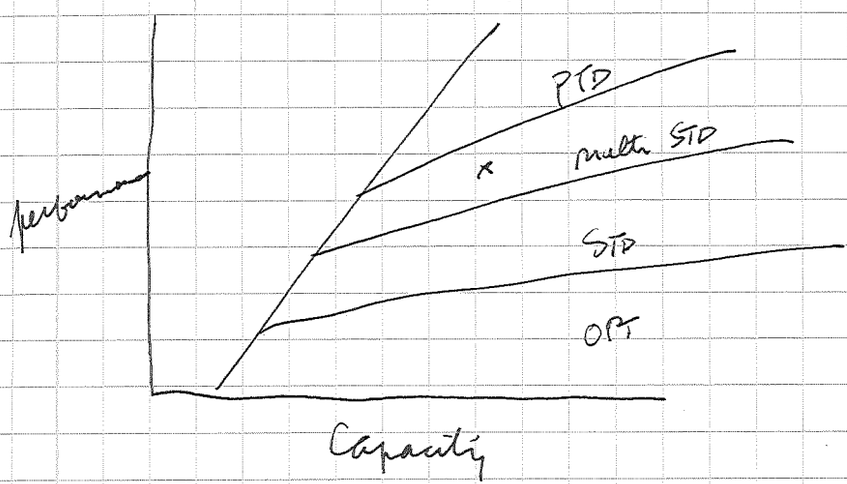
who is CDC contact

availability within 30 days for 1 CCU

UC03 - Emulex QBus - SCSI adapter
MSCP

3/13 DEC





10-20 Mbyte range - DEC shooting for

PTD problem - individual actuator for head for tracking

Optical - write once available 2-3 yrs. MOSK
1-2 Gbyte, slow 5 Mb/s, very slow access

PTD IBIS 1.4 GB 14" winch 32 heads - 100-200 shipped

Fujitsu

Dual porting -

BI - high speed IO bus

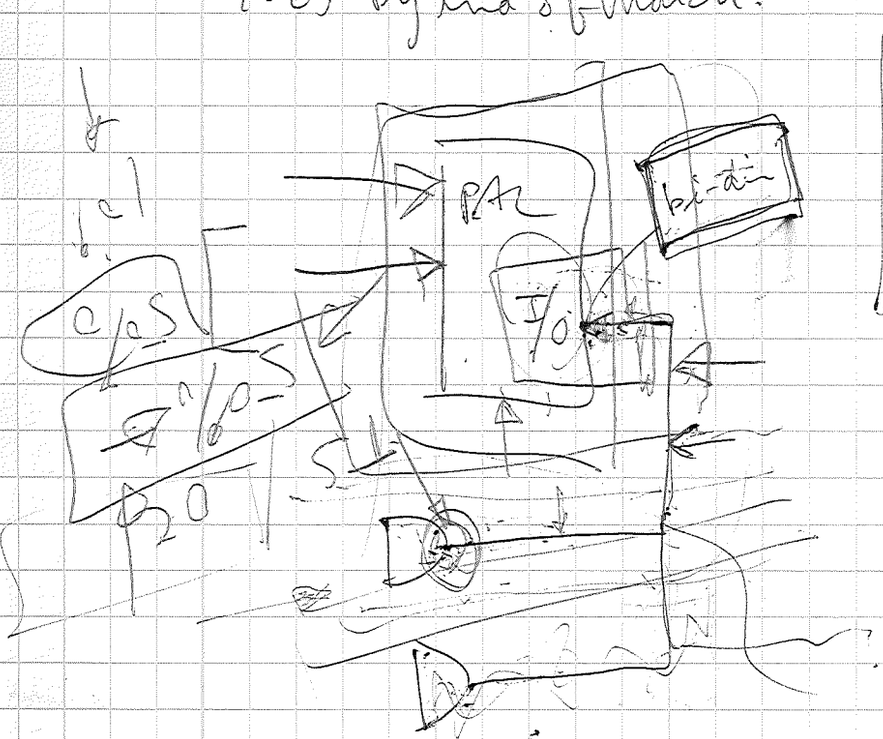
CI - 80 Mbit/sec

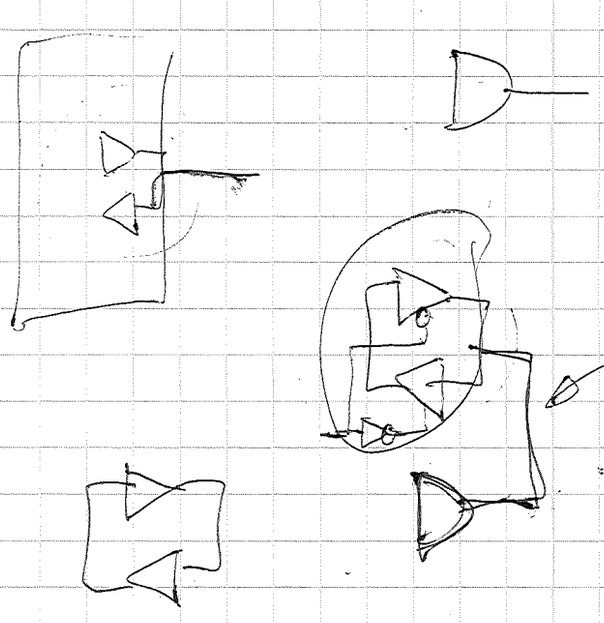
K Srivastava
Ed Gast
} DEC dists

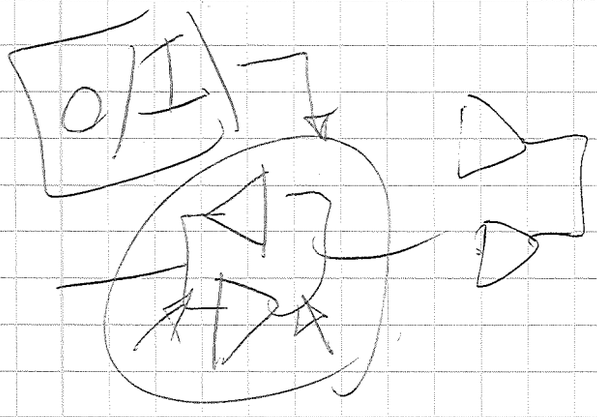
Valid 3/15.
Ethernet.

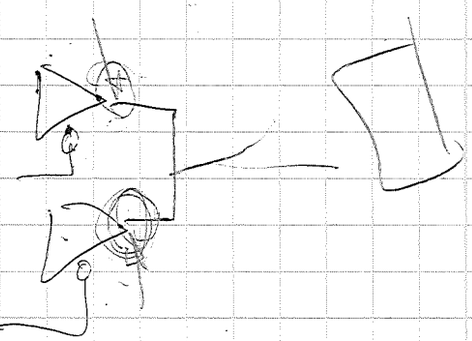
TCPIP ported

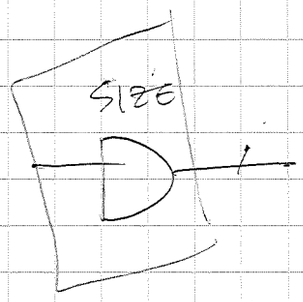
7.25 will support TCPIP, but not ARP
7.25 by end of march.

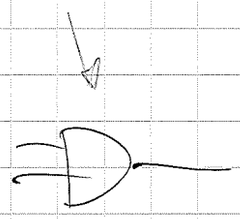


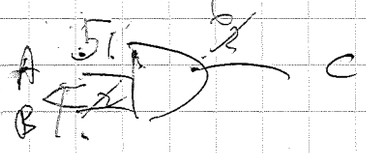


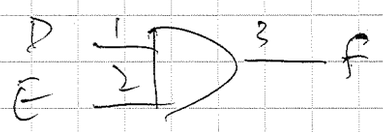


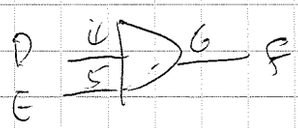


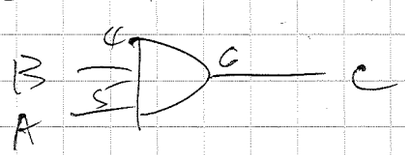

size

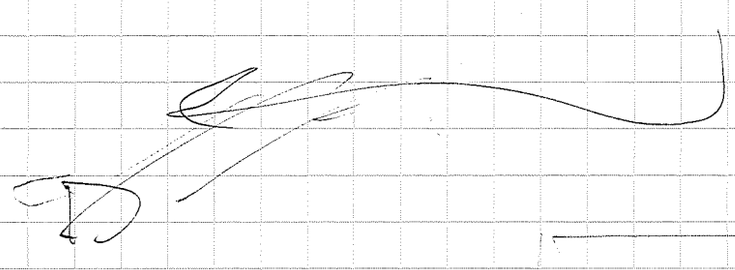


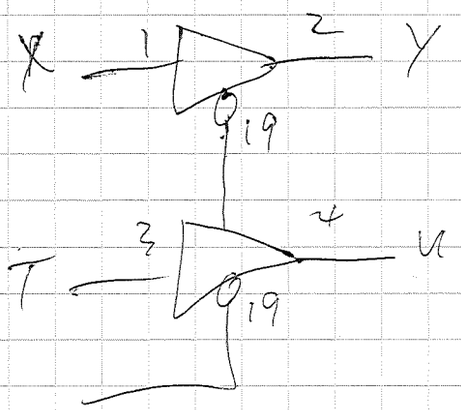

A
B
C

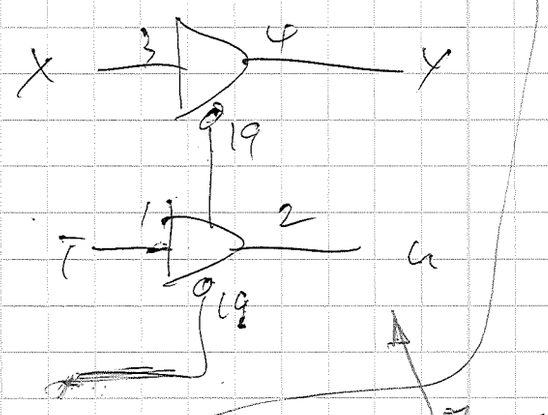

D
E
F


D
E
G
F


B
A
C




X
Y
T
U
19


X
Y
T
U
19
7.25?
7.4

XEBEC

CDC drive.

Jeff Lesener (tech support) 301-992-7377

Starter Kits controller - drive
Evaluation unit

Production volume in June.
List ?

Emulex

Write - buffer control : starts write when full

read - starts SCSI after 1st block.

buffer size - need 20KB for 10 mbps

ECC - retry once, then correct, takes 4 revolutions.
Can be turned off, but will get hard error and no data.

3/21

Patent requirement:

1. ECC description

2. buffering / synchronization

- individual within each controller
- across all controllers.

3/25

Questions for Gundlex:

1. Must have buffer empty, buffer full flags

2. Can buffers be filled from SCSI, while being drained to drive (write op), Is there a performance degradation for this mode of operation.

3. need flow chart of R/W op.

3/28 CDC 8" drive

368 MB 15 MHz in production in 90 days. July

240 MB	10 MHz
515	15
804	24

MTBF 24K hrs.

SMD-E interface

media - oxide thin film heads

2:7 encoding density ↑ requires 11 bit ECC

30 Kbyte/track Standard. ⇒ eq to 9" drive.

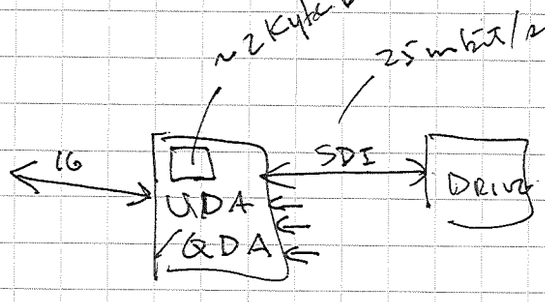
dual port selectable

$10/MB 8"
12/MB 5¼"

David wants

1. Status on SCSI & indicate done etc
2. Timing (reference diagram).

4/19 DEC



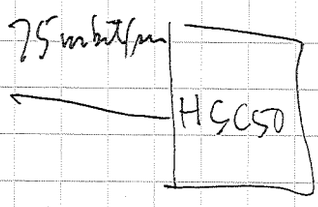
450 RA60 ~~170MB~~ R 250

QBUS – 4MByte/sec burst mode

1 sector/track ⇒ 3% of surface

RQDX-3 controller in same. 1 of 4/412 drive Qbus/412 or ESDI

H



Barry Rubenson Colorado. architect.

DEC disk controller chip. 16 bits / NRZ serial
Pheonix (?)

4/10
CUST4

✓ 1. ECO

✓ 2. termination flop

✓ 3. clks

✓ 4. Zipper — add branch; add abort; add ZOP; add buf ZOP; add nexus connect

[OP] ✓4, [ZOP] ✓

~~5. muxes~~

✓ 6. change GBUS ACK delay from 100 → 150 ✓ add 150 delay to lib

✓ 7. ~~fifo clks allow diff delay lines~~ FIFO clk - allow clk hi phase shrink.

✓ 8. delay Rdata parity check, ~~move check to LLRP 5A~~ [RDATA] ✓

X 9. csload while run

5. MUX — IF MUX ✓, OF MUX ✓ — [↑OF] 4 ✓, [↑QTR] 4; GBUS OUT ✓ [GBUS] 4; ADDR IN ✓

U6-8	UC CLK
U3-3	MCNTR CLK
U3-6	DP CLK
U2-3	SEQ CLK
U2-6	UW REG CLK A
U2-8	B

✓ 15. pullup split

✓ 16. RESET split

✓ 17. RDATA check leave [RDMA] ✓ [ZOP] ✓

✓ 18. [CLK] ✓, [NOP] ✓

✓ 10. ~~[illegible]~~ generation new UC CLK L — CLK +90

✓ 11. add ~~HF~~ flag [RST] ✓

✓ 12. ... 37

✓ 13. COMP ERR

✓ 14. Catch OF OR

✓ 30 ✓ 26
✓ 37
✓ 32
✓ 14
✓ 13
✓ 3
✓ 6

4/18 from Ed Gask

42MB - 6MB/in² 85MB 10MB/in² by a factor of 4

by vendor
- 100 drives avg 10.5 defects
  - range 0-31 "
  - standard 5.85 "
  - mostly 0-21

within 48hrs
- 1099 drives 9 drives rejected > 2 new unmapped hard errors.

by DEC

4/24
CDC
Since Nov
- ST506 ~7000
- ESDI ~200 ~1000 this year

100 units 90 days lead time.

Zylogic
Xlnet
Interpan

4/29

Mostek FIFO
- 65 sampling
- 80 production
- 100 "

5/7 Tele Art B. Ackerman

1. TA will provide a boxed mechanical drawing. Clem will define connector pinning.
2. define location of connector J1.
3. '2566' on VALID ?
4. ~~Tom~~ Sladen at TA VP of operation. For checking signal naming constraints.
5. 'Special consideration' check with Ron Mosher, EE.

5/8 IDT

50	x 8		~~$~~ $87	25+
65			69	
[80]			53	
120			39	
16K x 4	45		$ ~~200~~ 200	~~187~~
	55		150	
	70		100	

5/10 ~~Seagate~~ CDC Jim Ousley

When III announced in Summer. Medium production in December.

$10/megabyte from 5¼, 8 & 10 $8-9/megabyte for 14"

$30-40/megabyte → 1.4 gbyte 'Hydra' 14" drive. 4 spindles.

5/10 TEKART

1. gen vcc gnd list of connectors.
   ≈32 per 14 pin.
2. separate ground for IC in database.
3. change - get new database for comparison
   get Δ file for incremental input.
4. crosstalk - ~~[illegible]~~ arrival & manual
5. Nam spec sheets.

5/15 LATTICE

16K x 4 since Jan'85 in production.

	1K	5K
35 ns	180	135
45	128	96
55	80	60

$30-40 in '86

GM in production

	1K	5K
25 ns	6.5	5
35		
45		

5/29

AST 61 available on 6/19
103 " " 7/19

5/30 Hitachi

Static bipolar	16K x 4	4th Qtr 85	production	25, 35ns
	64K x 1	3rd Qtr 85	"	25ns
CMOS	64K x 1	45, 55ns	in production	
CMOS	16K x 4	2nd Qtr 86	production	35, 45ns

		Compile	Package	Gscale	
(50)	Cmbd	3/1	.75/.75	.5/.5	3.2
(101)	UC	22min/21min	.5/.5	.5/.5	22 M

DATA CONN

XRE in Littleton

Nancy Hackerty 486 9681

Fujitsu Jon Vincent app. engr. local.

Mike Gamergl calif

8/7 Lattice

2/2yr old Public in spring

750 warm/wk →

GAL 15ns targeted non-funct.

8K by 8 static RAM

256

.05/1K hr/device

500 FITS → 100 FITS target

printed ↑ in one year ↑

NMOS 4K x 4	now at 500 fits	
DRAM 64K	1000 fits	
CMOS	150 - 100 fits	
256K	3% / 1000 hr/dev	
CMOS "	1%	

Couple of rows of redundancy & provide

.33 bypass recommended.

Micron

200, 250 ns 256

256 K FETs: 100 FITs 4000 - 5000 FITs

200 ns ≤ $2.0
150 ns $3.5
120 ns $?

} Volume being sampled.

Primus Steve Albino (mem group)
IBM
Nixdorf
Analogic

Grompson second source.

IDT.

Room pack

16K x 4 55 ns avail. now

AMD 8/21

29C101 sampling Nov '85, prod. March '86
4x cmos version of 2901C

29C10A sampling now. prod Dec '85

29PL141 fuse programmable, samples now, Dec prod.

29130 16 bit barrel shifter. sample april '86
need data sheet.

29331 16 bit seq. sample Nov '85, prod May '86

29334 4 port dual access reg. file sampling Sept '85
prod Feb '86

29117 sampling now, prod Dec
sep I/O version of 29116

Mitsubishi Fuji

18P8 generic for 16x family
need data sheet.

2901D ?

2901C-1

Micron 8/26

Gene Cloud (Application Engr)

# of defects leaving factory: hard
soft

4 bit check bits single bit det / single bit correct.

What happens when double bit error is detected
1. 'corrected data' = ? in general
2. corrected data written back ? in general

Scrubbing: supported only by CBR refresh?

R/W/Rmw - correction written back to mem.

CBR - half of 256K vendors.

double bit error 'garbled'?

32K 12 bit words

Detect HE by sensing ICC: 3 → 6 ma during correction.

2 grades ← no more than 5 HE.
no HE. (prime parts) 80% yield } little Δ price.

200-500 ~~1000~~ SE 150 ~~HE~~
250 HE 100 ~~SE~~

1M design will have error signal out.

best pins 1 & 2: is vcc pad.

BP 60 days from now, no shipping yet. done independently

Typ current spike 65-70 ma at RAS ↓ Vcc ↓
(due to ckt pre-charge) ~ 10-20 ns duration.

39 mf edge
.3 mf device.

IBM / ~~DEC~~? failure analysis
CRSY
HP not a major user. good, starting.

120 wks being sampled 8-12% yield

Speed from shrinking and processing.

AMP 8/26

Reasons: All 84 date code parts have potential insertion problem.

Boring: ?

TI

75	888	now	ALU	] package?
75	889	now	seq.	
	897	sept-Oct		
8.7	870	now		

Chris ~~Bob~~ Demonico applic engr in factory.

TI. 10/1

Frank Lasko Dallas

Interphase 10/7 competition: Xylogics, Cipher

Bob Stout
Tom Thawley (tech contact) at Interphase.
Dennis Drapin

Siemens

300 MB production units in Nov. 50K in '86

designed & manufactured in Munich.

- embedded servo 5400 tpi / in / down

our units mid December.
50 units Jan-Feb '86

$9/10 per MB.

1K-2.5K over 2 years

Micron. 10/14

Simm - no ECC, page mode only.
ZIP - both

150ns 50% yield
120 9-20

1 meg with ECC Start of '86 80ns, 90ns

Skinny in DIP

TI 10/15

Bit slice Testing
development - bus contention check
instr - simulation & HW.

Production - functional testing?

Customers IBM, Data
Wang

Inmos

Q1 84 600 fits electromigration ~80 operating hrs.
Q2 260 fits

Q4 84 metal mach 3 1&2
42 fit — 360 fits nucleated stress growth

8410 worse, 8416 stops.

1985 reliability sym

8440 thru 8516 ~~<100 fit~~ 10% bad can be tracked.

Beyond 8516 less than 15 fits.

IBIS 11/13

60K 1.5GB

Interface ISI, IBIS drive interface

VME Bus structure suggested.

No controller, but drive interface easier design.

~~600~~ 750 shipped by end of year. 1st ship '83

Media proprietary & no second source.

Head - ferrite & T.F. heads, going towards T.F., vendors.

~~mech~~ mechanical 20
servo 6
R/W 4
} IBM, Burrough, DEC

Systems big

MTBF — parts count, mil spec

HDA 80K MTBF

12/13 Lattice

140 FFTs currently.

Int. Goal = 100 FFTs.

8K x 8 600 mil 28 pin.

12/13 Micron options:

1. 256 ECC (64x4) not a dead issue, only 150ns, Steve estimates to be $5 range.
2. 1 meg (256x4) in CMOS, ECC & 100, 120 ns dip in fall zip in march
   has pin for row strobe
   and " " reading out data
3. ~~1~~ 256 (64x4) page mode, 2 new mask: x1, x4, ~~with~~
   Can be in 20 pin zip & compatible later 1 meg zip.

   Tmc ~~wants~~ (or someone else) can funds for tooling. (10-12 wks.)

matrix hd review 4/1

1. Connector discussion - reliability / backup strategy.
2. Heat dissipation - need study.
3. repair strategy
4. test strategy
5. error status sw readable
6. cable termination // instead of serial is to speed up signal prog. Q1. do we need it
   Q2. current flux goes up for it.
7. I/O big 32 20 pin to edge : cost pin & xcvrs.
8. get amp rating from Amp on pin.
9. cm socket must be removable in layout.
   Brandy ~~buffer~~ preferred by TC
10. need specs

4/15

→ get machine spec

Bob

1. Status Panel mechanical
   Brackets drawing out at vendor
   10 on order

Status Panel Electrical design status.
5 bds in house, parts in house

2. PMP — schematic — design service
   spec — /u/Bob
   Part listing — /u/Bob

3. Cable tests — Notebook — schematic
   — spec
   — SW Bill

5/7 FB design review.

1. Zoom & PAN: can be fixed to preserve alignment?

2. Frame Grabber

5/8 Tech Dir Steve Manning

profile of Tarc - will draw high level people recommended

insolation

1 page of globe 19K - 400+ response 2 sundays, or a week later weekday.

instant response

~~Ad~~ Temp

1. $35-50/hr 45
2. on site sec. clerical help filtering & track & schedule
3. ad budget. 10-20K
4. acc to reg.
5. min 30 days, - 90 day.
6. all info flow thru reg.
7. next week start 5/19

1. get more resources
2. document
3. UCLID resource.
4. Data I/O — terminal Dom pix 3rd floor. (Dom)
5. handling - process
6. Quantum-fast cabling
7. Ted's mechanical design review.
8. Ship requirement.
9. PMP before shipment.

32K pretty → 64K pretty 6/1

Ship 3 x 16K 6/15 multichart + E

Mech. Design

1. Clerical errors & vendor errors: update prints

2. Design issues: fittings, legs affecting them.

→ Check HW-crew mailing list.

Status meeting 5/16

1. 1/8 machine ECO

UC - new pal 16 wires
Buf - 1 wire
BP - 1 wire
Zrig - pal ECO, 8 wires, NEWS wrapping? [DAS]
NEX - pal ECO, 9 wires, all news, 2 ECOs

2. Drive II cabling, [DAVID]

3. diode in power controller? [Bill]
Cabling

Thermo shutdown [Bill]

4. ship-
Spare refinement for customer machine
New matrix, old matrix?
Temperature & voltage margining.

5. ~~Skins~~ Marked up doors in 1 week. Review prior to incorporating in drawing.

Review list early next week. Monday afternoon.

7-12 wks. vendor time

6. NGX

7. BIBI 6/22, prints by 6/21, back in a week.
Debugging code & procedure.

8. Gig health chk help

9. Bill & DAS close out 3x

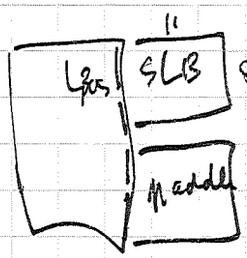
10.

Symbolics

G, I-machine

SW, FB

G-machine - same bus & mech. 5% mode change
36xx → gateway
Fewer parts same



← 1 MW mem bd
Console

LBUS changes: DMA added
interrupts more supportable

3600
40
70
> MC

45
75
> IFU, DMA

G - DMA

G → proc
Console
1 MW
FEP IO: FEP
Disk
Ethernet
serial
calendar

LBUS
SLB
SLB

Main address space 8mb → 16 mb

30K / 100's

Config: ① 3620/3610

10½" 8½ × 17 × 25

rack mount

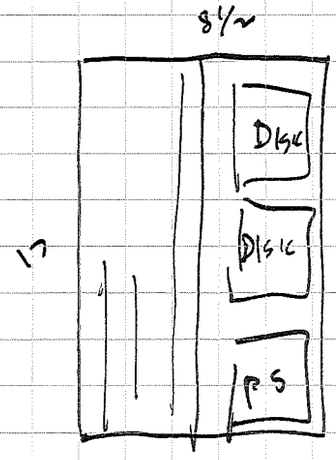
2 5½ Win or 1 5¼ Win + 1 Cart. tape.

180MB

---

base machine

3 SLB expansion



Available Oct. 86

② 3650 same box as 3640

17W × 32D × 30H

2 8" disks or 1 8" + 1 5¼ or 4 5¼

(no tape)

---

base

8 LBUS + paddles

6 SLB

Available before Oct '86

I-machine. new arch. new low level code
similar packaging.

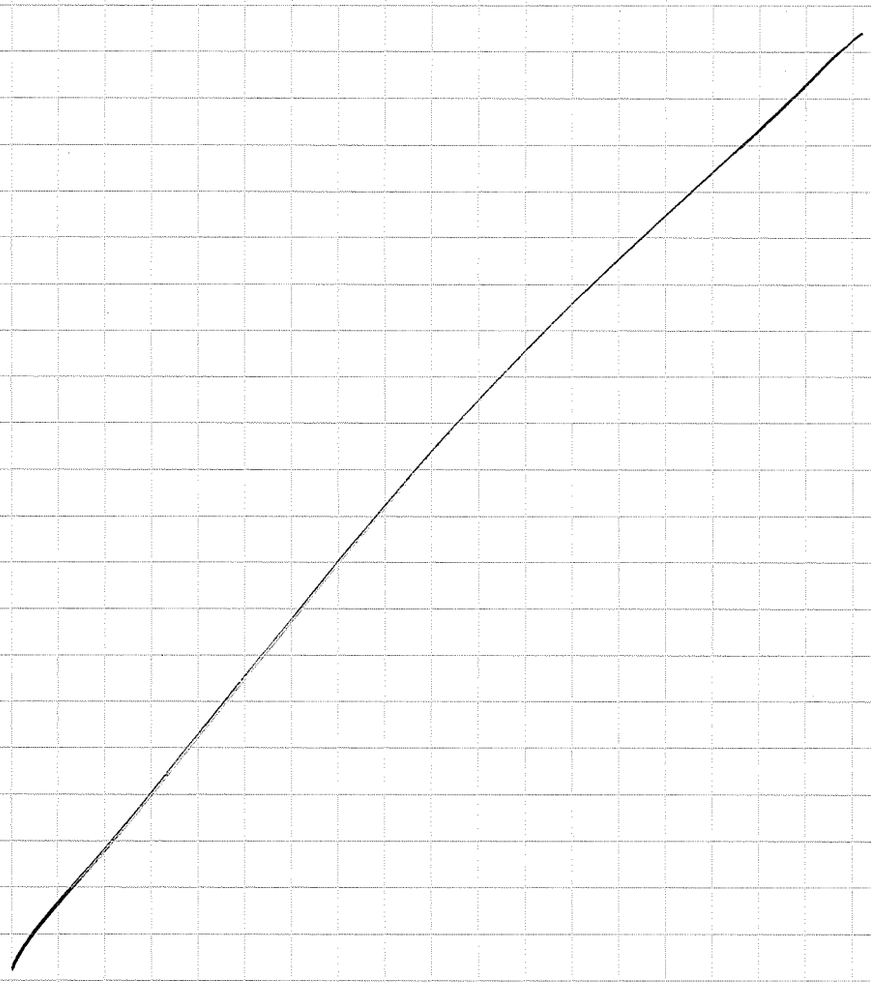
Single chip
↳ Single bd machine, desk top
Box machine

I bus

I/O port VME

28 bit physical addr space planned → 32?
36 bits wd → 40

Single bd machine summer '87
3–6 × performance



End of week - clean up all old prints

CMOM 5/20

Personnel: where we are, where we are going.

Machine usage:

Wed.

5/23 Status meeting.

1. BP eco - need to verify
2. Fpga eco affects cable document Bee.
3. Eco need diag running.
4. Plug ID verified.
5. IBK problem: BP, cross Q cable, lost bd 2 at least.
6. BIOS schematics ready by 5/23. db to go out 5/23 incorporate reg change, 5/28.
7. Diag - Sandy is full of shit.
8. Prism II activex item David.
9. NS wrap
10. Mtg GCO, d UC
11. bd status to TC

70 MB + cab etc	11.9 K
474 MB + cab + controller	26.5 K
140 MB + cab	15.9 K

68020 upgrade & replace	14 K
+1 MB	15.5
2 MB	19.9

Graphics 2310 — 14.5 K — ~20% degradation

System VLD431	69.5 / 78.
4426	$9 / 71.5
Ethernet	4.8

3 weeks → 1 week.

5/30

1. Nexus - multi host on 1 multi wire only
   - Rev 3 wire wrap has multi uC problem.

2. Bd checkout - ~20 out of ~50
   - get all new bds back in for burn in.

6/10

What needs to be done to release matrix.

1. B.P. changes.
2. uC interface
3. System timing
4. System reliability

System clocking scheme (Bob)
Backplane (Bob & ?)
System reliability (Dave & Bob)

6/12

1. Charles will write device driver & interrupt handler.
2. Charles will kick people off to allow BIBL debug.
3. Dave owns spec & code for Text routine.
4. Weekly meeting at Thursday 1:30
5. BISC chip not in house.

6/19

1. BI req R/W capability
2. device drivers dependent on ultrix source.
3. extended will have written 2 days.
4. /cm/BIBL ECO & log.
5. available next week.
6. Common Lisp problem.

6/25

1. [redacted]: still can't compile source, bugs
   = still don't have device.
2. Get BIIIC (new?)
   BIIC insertion — Angat
   — Dec
3. Test spec held off until debug schedule, by 7/3.

7/3

1. init — load device type BIIC
   — BI state machine
   RD/WRT BEIC reg done.
2. extraction / socket Angat
   Glow Dec

7/10

1. driver written, not tested
2. load device type not at IC during power up.
   reset mode — state machine in idle
   R/W sta reg — don't work but came no error.

7/17

1. driver done, 1st pass
2. Can now R/W status correctly, bug was missing ACIC
3. find out if new decode can be gotten.

7/24

1. Highesting W/R FIFO, parity OK.
2. discard not working completely.
3. get new prodesfrom DEC.

meeting next Mon 4.

8/8

DAVES vacation 8/2-16

Will get PROM code running
& 2nd BIBI GCO'd & mips.

8/12

1. 16 Mbyte machine. → 4 bds   1/8
40 mips

8/17

1. Wait States ~~was~~ not working. } ~~HW~~ need: to eliminate system crash.
2. read seems to be
3. Count.

next week get Mike's diag working, loop back
& NBRCOS help.

Following week get PROM code running
& 2nd BIBI debugged.

→ get HW help
→ keep 8200 for a while

9/29

Massively Parallel competition
DAP - ICL based. current
HP, DEC, IBM - 6-12 mon
MPP - original version

Documentation

Agenda to nail down
- General purpose life
- realistic product cycle

	Product life cycle	Cost/performance debbie factor	
Rolf	4-5	10	(high)
Jim	4	?	

40 80 160 320 16K mx

87 88 89 90

Front end
- Should there be a single? - Rolf

Small machine 150

4 bd. - host ~~100K~~

ASI. 11/4

- 4 layer / section.
- routing is manual + auto
- placing & routing single section — 1 wk
  — 1 day / incremental change
- complete bd routed, 2 more days.
- additional wks for artwork plot spec
- plot will take 2 days. Boulevard, Wise laser plotters.

Break pt.

update - delta file
feedback - auto generated.

35K $55/IC → 700 IC equivalent.

4 wks. to artwork, anticipating 3/4 incremental changes.

Per mid-IC vacation for design.

$500/day $2500 — feasibility.

BP. 3-4 wks.

Kan Ex. 11/4

- section routing, mostly manual.
- section duplication - not clear
- 4-6 layer / section estimation
- 2 separation schematics.
- merge at photo plotting.
- 2 netlists gen & chk.

- 1 to 2% manual routing.

- running 1 plot ahead

- need extended mem station

- 4 designs
- slot open within 1 wk.

button in Mississauga for BP fab - George

AMP 11/5

- gnd pins wants to be on short connector pins.
  ? - 1% inductance.

- 5'-1 limit for thickness.
- ~400 mV gnd bounce anticipated.

11/6 schedule review.

Chip - 125 in house before Thanksgiving.
after 500 by Jan
2000 by Feb.
4.5K by March

test requirement - delay in system
- lots of routing (high bd)
need meeting

Bd - split pins
Width pins waiting for 64
System timing - need meeting.
need schedule -

Elect/Mech = power supply spec

UUC = host boards

Nexus — need body

Sprint — HW emulators?

SW = middle of planing.

Display — looking at megabit video rams.

Assessment — General purpose computing
FP
Standard algorithm & benchmarks
Fortran?
3rd party SW

Rem Ox B.P.

cnet conversion	1 day.
body	1 day
~~Pad~~ bd physical dr	1 day
placement, send check drill hole	1 day

} 4 days.

→ input change

Advanced Lam, NT, precision Lam.

Start monday.

---

1. route subpanel – copy net by net
   200 copies / section ⇒ 24 hrs / section.
   – adv. can check whole database.
   = net list – only one –
2. " " – duplicate section
   can't check whole database
   precaution – keep section on isolated layer.
   – net list – subpanel + incremental.

Routing – problem

Return-Path: jim
Received: by Godot.Think.COM; Tue, 27 Jan 87 07:28:19 EST
From: jim (Jim Bailey)
To: clem
Cc: jim
Subject: Re: announcement machines
In-Reply-To: Your message of Mon, 26 Jan 87 14:38:14 EST.
Date: Tue, 27 Jan 87 07:28:17 EST

yes. let's get together today. i had expected an all-day with a customer, but they canceled, so any time is good.

I envision a mix of alpha and beta machines for the introduction. For the festivities here, I expect we'll have more than four quadrants (alpha plus beta) running. I would like to bring four quadrants, spread across two cabinets, to California.

Obviously, as many of the quadrants should be beta quadrants as possible. Can we plan on having two? Then we will stuff whatever floating point sets we have into one of the beta systems. The disk will also go on one. I'd like floating point and disk to be separate; hence the desire for two beta quadrants. If we have two beta quadrants, the other two would be alphas.

The goal is to have four or five applications running, and to swap them among the quadrants during the week. We don't have to show all applications running at beta speeds all the time, as long as we have run them, and we know the timings.

I assume a bunch (6?) of front ends. We need one or two highly visible Vax's, but the rest can be 3600's as I see it right now.

11/7 AST

BP.

BP
39.9K

BlueBell pgm. do BP.

1. LISPm
2. Wed. 3pm meeting.

AST — up to 12 — up to 50 (?)

quick turn — 5-7 days. — 10-15 — 15-20

Qty 5-5

matrix 1558 ~~1169~~

~~1200 (?)~~

Nitex 1134

Uc 899

(can do Contract imp.)

1. meeting
2. HW Special

6 ~~demos~~ applications

1. doc retrieval off disk — Steve Smith
2. Molecular dynamic — FF — Bernie
3. Fluid Flow — FF — Goldy
4. VLSI sim, big one — Steve Daniel
5. Object identification — Lew Tucker
6. Seismic application — Bob Womsley

min of 4

FF - get benchmarks for all app.

min = Multitasking.
= 32K beta

Triad 11/12

Split database

Numerix 800TC eq. 8+2 layers. 24 x 24 wks

Calay 2 mbyte 20 MB drive.

Duplication - .

Rolf's sim meeting 11/12

Sprint chip timing spec needs to be reviewed

Stud chip needs timing spec — when from?

Beta matrix simulation — need netlist & pcb.

Release matrix

1. Wietek timing needed
2. Generate timing for Sprint
3. Generate neutralize signal for Wietek.
4. design review on Monday
5. Timing review on Wed pm.

Backplane.

1. layout in progress
2. Fab house

} 1. design rules
2. layer ordering
3. screen

Extender.

1. clock ~~driver~~ buffer
2. ~~pipeline~~ mapping.

UC.

Fabric design.

1. ~~mem~~ handling Jim.
2. 16 bit bitmap Jim I/O related. } by Wed.
~~3. 12/20 + 16/16 ~~
3. Width bound check
4. Drag Hold Jim.

80% wire wrap ± 20%

→ Reference from IDT. 1,900 ma Worst case

EDI ~~Mem~~ CMOS 1,100 ma " "

32K x 8 SMD 30% hit on PCB density.

Adapter bd.

Zero Insertion - Intel plug in from Toyocomm in progress

~~Extender~~ New WW bd.

Material

1. beta chip test bed LISPM / HBI / NGX

2. additional LISPM possible Mongo
HBI
WCS NGX

3. T.C. - assembly & testing.

Personnel

1. Wire man/tech Rich to get back to me.

Space

1. Stockroom to expansion area.

INTEL 1/23

ASIC

1. both gate array & standard cells. 1.5 micron, chip for 2 yrs.
Switch into 1.0 by end of year.

2. gate array, joint with IBM C-4 technology, licensed by IBM

1/28

Mech

Ted 1. Card cage, redrawn done, waiting for P.O.

Ted 2. Power supplies, main +5, 250a
-5, 30a
, nexus +5, 30a
-5, 2a.

10-20 by mid Feb
vol by end of Feb.

Frank 3. Power Controller upgrade
2/21 with proto

10 built by mid Feb

Ted 4. Doors, started design & sample done

4 in ± 2 wks.
Vol than +6 wks.

Lock problem?

Ted 5. Chassis
- add pans for shield installation, design & drawing done
- T frame change " " , not done, redo done
- new finish to match for FCC " " " "
- top cover, need gnd. " " , 2 wks.

need help 6. Adjustable legs
1. tipping — plate
2. leveling — adjustable wheels?

design drawing done in 2 wks

Tom? 7. Cabling — I/O
talk to Potter

Ted 8. Thermal
- paper evaluation, 2 wks
- data measurement
- adjustment redesign

9. Test — shield
plan?

22 working days. from db to boards; no change

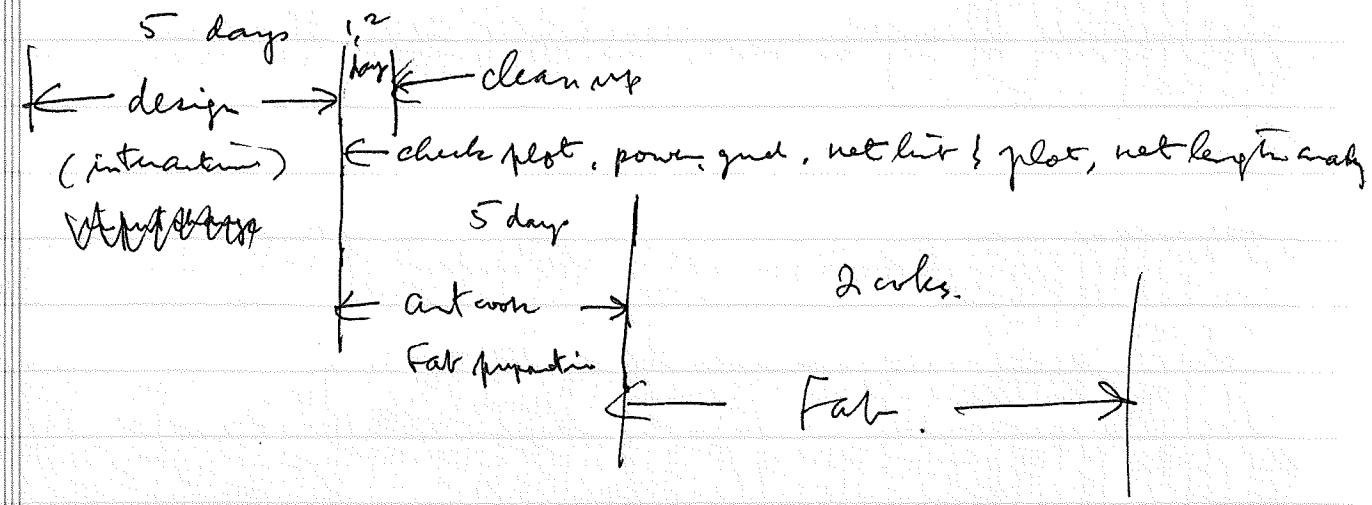
↓

25

4-9 for initial build.

2 wks for more bds.

22-day flow



- quote nexus
  uc
- breakdown 22 days, including change
- identify designer

404 938 9387
John Sanders

Symbolics
577 7500

Larry Coppenreth

cutler → Symb. → lay off
proj admin

- manager microx-1
- manager new system development at Symbolics
  - took too many things into own hand
- get things accomplished, step on toes (peers)
- no info on technical.